

ES1651.1 Carrier Board User's Guide



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1 Introduction

This User's Guide contains the description of the ES1651.1 Carrier Board. It consists of the following chapters:

• "Applications and Features" on page 6

The introduction contains an overview of the characteristics of the ES1651.1 Carrier Board and also includes a block diagram.

• "Hardware Features" on page 10

This is where the properties of the ES1651.1 Carrier Board are described in detail. These are:

- "Carrier Board for Piggybacks" on page 10
- "Synchronization Bus" on page 10
- "Crankshaft Angle Clock Bus (CAC Bus)" on page 11
- "Generating an Interrupt" on page 15
- "Inspection and Versioning Data" on page 16
- "CAN Interfaces (Optional)" on page 17

This section contains information on the CAN interfaces.

• "Configuration" on page 20

This section contains a description of the configuration possibilities of the ES1651.1 Carrier Board and their presettings.

• "Addressing the ES1651.1 at the VMEbus (SW1 and SW2)" on page 23

This section describes addressing the ES1651.1 at the VMEbus.

• "Installing I/O Modules" on page 26

This section describes how to assemble I/O modules on the ES1651.1 Carrier Board and any necessary preparatory steps:

- "Assembling the Front Panel to the PB4350XXX Module" on page 26
- "Mounting the CAN Transceivers" on page 29
- "Mounting the I/O Modules" on page 30
- "Pin Assignments and Display Elements" on page 34

This section contains a description of all connectors on the front panel and on the board as well as the meaning of the LED displays. • "Technical Data" on page 40

contains the technical data of the ES1651.1 Carrier Board.

Note

Some components of the ES1651.1 Carrier Board may be damaged or destroyed by electrostatic discharges. Please keep the board in its storage package until it is installed.

The ES1651.1 Carrier Board should only be taken from its package, configured and installed at a working place that is protected against static discharge.

Note

The components, connectors and conductors of the ES1651.1 Carrier Board may carry dangerous voltages.

These voltages may even exist when the board is not installed in the VMEbus system or the VMEbus system is powered off.

Make sure that the board is protected against contact during operation. Disconnect all connections to the ES1651.1 Carrier Board before removing the board from the VMEbus system.

1.1 Applications and Features

The ES1651.1 Carrier Board acts as a carrier board for up to four I/O modules in VMEbus systems. All modules of types "PB4350XXX" and "PB1651XXX" can be used in any combination. An SPI control unit realized in the FPGA of the board converts the parallel data flow of the processor into a serial bit flow for the SPI interfaces of the I/O modules.

The ES1651.1 Carrier Board has a crankshaft angle clock bus for testing engine ECUs in LABCAR projects; this can be used to synchronize I/O modules with a central crankshaft angle clock for speed-synchronous signal acquisition and signal generation. The crankshaft angle clock bus is routed to the 9-pin Sub-D connector on the front panel of the board so that the crankshaft angle clock can be both supplied externally as well as routed to the outside.

Synchronization Bus

The ES1651.1 has a synchronization bus to synchronize the I/O modules of an ES1651.1 Carrier Board with each other. It consists of four lines which can be configured independently of each other. The bus is also routed to the 9-pin Sub-D connector on the front panel of the board so that the signals can be

supplied externally or routed to the outside to synchronize I/O modules on other carrier boards. The synchronization lines can also be stimulated from within the simulation model.

CAN Interfaces

There are two identical CAN channels on the ES1651.1 Carrier Board for connecting the board to the CAN bus. The transceiver functionality is realized on piggybacks so that, if necessary, different transceivers can be used than those intended, i.e. than the PCA82C251 transceiver by Philips for high-speed CAN applications ¹ and the MAX3055 transceiver by Maxim for low-speed CAN applications².

The ETAS PB1651CAN1 transceiver module is a combined high-speed/low-speed CAN transceiver module³ with galvanic isolation of the CAN channels. Relays are used to toggle between high-speed and low-speed functionality. The CAN controller functionality is realized in the MPC555 processor of the board which has two CAN channels on board.

VMEbus Interface

The ES1651.1 Carrier Board has a VMEbus slave interface and reacts to "A24 non privileged data access" accesses (VMEbus address modifier 39 hex).

The position of the 64-kByte VMEbus address space of the board can be set either dynamically or statically. Data is exchanged with VMEbus master boards via a 32-kByte DPRAM. The board can trigger interrupts at the VMEbus.

Inspection and Versioning Data

Inspection and versioning data of the board are stored in a serial non-volatile data memory. PB1651CAN1 transceiver modules also have serial data memories for version and inspection data.

Processor

In addition to the CAN channels listed, the MPC555 processor of the board also has a 448-kByte ROM memory which is large enough for program code and data; this is why the optional external ROM memory is not assembled.

- ^{1.} High-speed CAN systems (data rates between 125 kBaud and 1 MBaud) are used e.g. for engine and transmission controls, ESP, ASR, ACC and ABS.
- ^{2.} Low-speed CAN systems (data rates up to 125 kBaud) are used in the field of convenience electronics.
- ^{3.} The terms fault-tolerant CAN and low-speed CAN are synonymous.



Fig. 1-1 shows the front panel of the ES1651.1 Carrier Board.



Front Panel of the ES1651.1 Carrier Board

1.2 Block Diagram

Fig. 1-2 shows a block diagram with all important functional units of the ES1651.1 Carrier Board.



Fig. 1-2 Block Diagram of the ES1651.1 Carrier Board

2 Hardware Features

This section contains a description of the different hardware features of the ES1651.1 Carrier Board.

These are:

- "Carrier Board for Piggybacks" on page 10
- "Synchronization Bus" on page 10
- "Crankshaft Angle Clock Bus (CAC Bus)" on page 11
- "Generating an Interrupt" on page 15
- "Inspection and Versioning Data" on page 16

2.1 Carrier Board for Piggybacks

The ES1651.1 Carrier Board is used as a carrier board for I/O modules in VMEbus systems. I/O modules are available for various tasks, such as the generation and measuring of ECU signals in real time.

All modules of types "PB4350XXX" and "PB1651XXX" can be used. This means that the LABCAR test system can be equipped both with the standard I/O modules for the ES1651.1 Carrier Board (VME system) and with the highly precise I/O modules for the ES4350 Carrier Board. Up to four I/O modules of both types mentioned above can be used per ES1651.1 Carrier Board.

The I/O modules are connected using ribbon cable. There are four connectors on the ES1651.1 Carrier Board for this purpose. For more details on how to assemble I/O modules, please refer to section 5 on page 26.

2.2 Synchronization Bus

The ES1651.1 Carrier Board has a synchronization bus for synchronizing

- the I/O modules mounted on the carrier board with each other,
- I/O modules with the carrier board,
- I/O modules with other I/O modules which are installed on other ES1651.1 Carrier Boards or ES4350 Carrier Boards in the same or other VMEbus systems,
- with other external hardware which can generate or interpret the relevant synchronization signals.

The synchronization bus has four identical synchronization channels. A block diagram of a single channel is shown in Fig. 2-1.



Fig. 2-1Block Diagram of a Synchronization Channel

The front panel connector can be configured as

- an input which provides the synchronization signals for the carrier board hardware and the I/O modules,
- an output which provides the synchronization signals for external hardware

or can be disconnected from the synchronization bus.

Internally the synchronization bus works with 3.3 V digital signals. To reduce interference sensibility, the signals are transferred to and from external hardware with 5 V digital signals. The direction of an individual synchronization channel can be selected independently of the other synchronization channels.

The input and output stages are protected against overvoltage from -14 V to +19 V (with reference to VMEbus ground).

For more details of the input and output stages, please refer to the section "Technical Data" on page 40.

2.3 Crankshaft Angle Clock Bus (CAC Bus)

The ES1651.1 Carrier Board has a crankshaft angle clock bus (CAC bus) for LABCAR projects which include the stimulation and testing of engine ECUs bus (CAC bus).

Like the synchronization bus, the CAC bus is also connected to the I/O modules and the FPGA of the carrier board. It is connected to I/O modules which are assembled on other ES1651.1 Carrier Boards or ES4350 Carrier Boards, or to other external hardware which can provide or process crankshaft angle clock signals via the 9-pin Sub-D connector on the front panel.

The CAC bus can be driven by the CAC generators on ES1332.1 and ES4320 boards (an I/O module for CAC generation is currently under development). The crankshaft angle clock cannot be generated in the FPGA of the ES1651.1.

The CAC bus of the ES1651.1 consists of the following three signals (refer to Fig. 2-4 on page 14):

- CAC-SYNC signal: Synchronization signal for 0 °CA
- CAC-CLK signal: The actual crankshaft angle clock signal
- CAC-DOR signal: Signal for displaying the direction of rotation

The following two figures show block diagrams of the channel for the synchronization signal (Fig. 2-2) and the CAC signal (Fig. 2-3) respectively. The channel for the direction signal is identical to the channel for hardware synchronization (see Fig. 2-1 on page 11).



Fig. 2-2 Block Diagram of the CAC Bus Synchronization Channel





- an input which provides the CAC signals for the carrier board hardware and the I/O modules,
- an output which provides the CAC signals for external hardware

or can be disconnected from the crankshaft angle clock.

The input and output stages are protected against overvoltage from -14 V to +19 V (with reference to VMEbus ground).

Internally the synchronization bus works with 3.3 V digital signals – the levels of the output signals of the CAC bus on the front panel are shown in Fig. 2-4 on page 14.

The CAC bus inputs can process two types of CAC signal:

• The combined CAC synchronization and clock signal as generated by ES1332 boards (see Fig. 2-5 on page 15).

This signal must be connected to the pin of the CAC synchronization signal as well as to the pin of the CAC clock signal of the Sub-D front panel connector for this purpose. In this case, the "Input ES1332 CAC" option must be set in the option box "CAC Port Mode" in the "ES1651-CTRL" RTIO element of the ES1651-RTIO integration. This results in the switch at the output of the 7.2 V comparator (Fig. 2-2 on page 12) and the switch at the output of the 2.2 V comparator (Fig. 2-3 on page 13) being closed.

• Input signals of the type shown in Fig. 2-4.

The signals are connected to the relevant pins of the Sub-D front panel connector. In this case, the "Input" option must be set in the option box "CAC Port Mode" in the "ES1651-CTRL" RTIO element of the ES1651-RTIO integration. This results in the switch at the output of the 2.2 V comparator (Fig. 2-2 on page 12) and the switch at the output of the 2.2 V comparator (Fig. 2-3 on page 13) being closed.

Note

The pin assignment of the 9-pin Sub-D connector is contained in the section "Synchronization Bus and CAC Bus Connection "SYNC & CAC" (CO2)" on page 35.

The direction of the CAC bus signals (input or output) can only be selected for the bus as a whole.





Fig. 2-5 Combined CAC Synchronization and Clock Signal (ES1332)

For more details of the input and output stages, please refer to the section "Technical Data" on page 40.

2.4 Generating an Interrupt

The ES1651.1 Carrier Board has eight interrupt lines which, connected via a logical "OR" operation, generate a common interrupt request on the VMEbus.

Each of these eight interrupt lines can be activated or deactivated using the software. If a line is activated, an interrupt request is generated by a falling signal edge on the interrupt line. The VMEbus interrupt handler then determines which of the interrupt lines was the source of the request.

The interrupt lines PB0_IRQ to PB3_IRQ of the I/O modules are connected to interrupt lines 0 to 3 of the VMEbus interface. The ES1651.1 Carrier Board also makes it possible to connect one of the synchronization bus lines to interrupt line 4 – this is selected using the software.

Interrupt lines 5 to 7 are not assigned to date.



Fig. 2-6 The Interrupt Concept of the ES1651.1

2.5 Inspection and Versioning Data

Inspection and versioning data of the board are stored in a serial non-volatile data memory which is addressed via the processor's SPI (Serial Peripheral Interface). The data can be read out via the operating software LABCAR-OPERA-TOR.

3 CAN Interfaces (Optional)

There are two identical CAN channels on the ES1651.1 Carrier Board for connecting the board to the CAN bus. The transceiver functionality is realized on piggybacks so that, if necessary, different transceivers can be used than those intended, i.e. than the PCA82C251 transceiver by Philips for high-speed CAN applications and the MAX3055 transceiver by Maxim for low-speed CAN applications.

The ETAS PB1651CAN1 transceiver module is a combined high-speed/lowspeed CAN transceiver module with galvanic isolation of the CAN channels. Relays are used to toggle between high-speed and low-speed functionality. A 120 Ohm bus termination of the high-speed CAN interface can also be activated and deactivated using a relay switch.

The relay switches can be controlled using the LABCAR-OPERATOR operating software. The CAN controller functionality is realized in the MPC555 processor of the board which has two CAN channels on board.

The PB1651CAN1 transceiver modules have a serial non-volatile data memory for inspection and versioning data which is addressed via the processor's SPI interface. The data can be read out via the operating software LABCAR-OPERATOR.

The block diagram of a PB1651CAN1 transceiver module is shown in Fig. 3-1.





3.1 Features

The PB1651CAN1 transceiver modules have the following features:

- Galvanic isolation from the VMEbus
- ±36 V on CAN_H and CAN_L
- Toggling between high-speed and low-speed CAN interface via relays
- The high-speed CAN transceiver is fully compatible with the ISO 11898-24 V standard
- 120 Ω terminating resistor of the high-speed CAN interface can be switched using relays

- Full support of the operating modes "Standby" and "Sleep" of the fault-tolerant CAN transceiver as well as error monitoring
- Switch technology for reducing electromagnetic emission and improving the electromagnetic compatibility of the CAN channel
- SPI bus EEPROM for versioning, inspection and maintenance data
- Automatic detection of the transceiver module with the LABCAR-OPERATOR operating software
- The bus lines CAN_H and CAN_L are each terminated on the low-speed CAN transceiver with 2.2 k Ω .

3.2 Pin Assignment and Signals

The CAN transceiver module and the ES1651.1 Carrier Board are connected using an 8-pin and a 16-pin connector. For more details on the pin assignment, please refer to the section "Connectors for CAN Transceiver Modules" on page 36.

4 Configuration

Fig. 4-1 shows the position of all connectors and switches for configuring the ES1651.1 Carrier Board - in addition to important components and connectors for orientation purposes.



- Fig. 4-1 Position of the Connectors, Jumpers and Switches (Component Side)
- 4.1 Configuration of the Debug Port Connections of the Processor (JPO)

JP0 Jumper	Meaning
set	Debug port connections
open	JTAG interface (preset)

Tab. 4-1 JPO Jumper

4.2 JTAG Chain Configuration (JP1)

Use the JP1 jumper to set whether the I/O modules are included in the JTAG chain or not.

JP1 Jumper	Meaning
Pos. 1-2	JTAG chain bypasses I/O modules (preset)
Pos. 2-3	I/O moduls are included in the JTAG chain

Tab. 4-2 JP1 Jumper

Note

The jumper at JP1 must be in one of the positions listed in Tab. 4-2. Otherwise the JTAG chain is open which leads to errors.

4.3 Boot Configuration (SW0)

The boot configuration is determined using the SWO switch.

DIL switch	Meaning	Presetting
1	Flash enable – determines whether the MPC555 Flash memory is activated or deac- tivated after a reset. OFF: Flash disabled – the system is booted from the external memory ON: Flash enabled	ON
2	Determines the base address of the MPC555-internal memory space OFF: 0x0000 0000 ON: 0x0100 0000	OFF
3	Boot port size OFF: 32-bit port ON: 16-bit port	OFF
4	Hard reset configuration word OFF: Configuration word is read by external data bus ON: The internal configuration word is used	OFF
5,6	Source for boot code OFF, OFF: Internal flash memory OFF, ON: External SRAM ON, OFF: Dual-Ported RAM ON, ON: External Flash memory	OFF, OFF

Tab. 4-3DIL Switch SW0 for Boot Configuration

4.4 Reset Switch (SW3)

Results in a reset of the ES1651.1 Carrier Board, but not a VMebus reset.

4.5 Addressing the ES1651.1 at the VMEbus (SW1 and SW2)

The ES1651.1 Carrier Board can be operated both in (standard) VMEbus systems with 96-pin backplane connectors and in VME64x systems with geographical addressing. With two HEX switches, SW1 and SW2, (see Fig. 4-1 on page 20), the board is addressed in the setting "0x00" in "geographical addressing mode" and in all other settings in the relevant address spaces.

	VMEbus
On-chip Register	0x0000
22 Byte	0x0015
Reserved	0x7FFF
/CSO (DPRAM) 32 kByte	0x8000 0xFFFF

Fig. 4-2 Address Map

Slot Position	Address	VME Interface (Control Register)
1	E0E000 - E0E0FF	256 bytes
2	E0E100 - E0E1FF	256 bytes
3	E0E200 - E0E2FF	256 bytes
4	E0E300 - E0E3FF	256 bytes
5	E0E400 - E0E4FF	256 bytes
6	E0E500 - E0E5FF	256 bytes
7	E0E600 - E0E6FF	256 bytes
8	E0E700 - E0E7FF	256 bytes
9	E0E800 - E0E8FF	256 bytes
10	E0E900 - E0E9FF	256 bytes
11	E0EA00 - E0EAFF	256 bytes
12	EOEBOO - EOEBFF	256 bytes
13	E0EC00 - E0ECFF	256 bytes
14	E0ED00 - E0EDFF	256 bytes
15	EOEFOO - EOEFFF	256 bytes
16	EOFOOO - EOFOFF	256 bytes
17	EOF100 - EOF1FF	256 bytes
18	EOF200 - EOF2FF	256 bytes
19	EOF300 - EOF3FF	256 bytes
20	EOF400 - EOF4FF	256 bytes
21	EOF500 - EOF5FF	256 bytes

In the "0x00" setting, the ES1651.1 Board maps 256 bytes into the A24 address space depending on the slot position. Depending on the available memory area, the 64 kB address space is then assigned dynamically by the system controller.

Tab. 4-4Slot Position and Address

Note

VMEbus backplanes can have a maximum of 21 slots.

The 64 kB address space is assigned statically with every other setting of the hex switches (\neq 0x00).

Switch Se	tting	Address Space	
0x01		010000 - 01FFFF	
0x02		020000 - 02FFFF	
0x03		030000 - 03FFFF	
OxFF		FF0000 - FFFFFF	
Tab. 4-5	Setting the	Address Spaces	
SW1	SW2		
4 2 0 E C	4 2 0 E		
Fig. 4-3	Switch for <i>i</i>	Address Setting	
SW1		SW2	

SW1	SW2
0x n 0	0x0 n
Address A23 - A20	Address A16 - A19

Tab. 4-6Meaning of the Switches SW1 and SW2

Example:

Required: base address A24 at 0xC20000 Settings: SW1=0xC, SW2=0x2

Note

The default setting is: SW1=0x0, SW2=0x0

5 Installing I/O Modules

This section describes how to install I/O modules.

Note

I/O modules of the type "PB1651XXX" are delivered with the front panel assembled; modules of the type "PB4350XXX" come with a front panel which is not assembled. If you want to mount a module of type "PB4350XXX" on the ES1651.1 Carrier Board, you first have to assemble its front panel.

5.1 Assembling the Front Panel to the PB4350XXX Module

•

Proceed as follows to assemble the front panel on a module of the type "PB4350XX":

Tighten the printed board brackets as shown



Fig. 5-1 Tightening the Printed Board Brackets

• Fasten the front panel with the hexagon head screws above and below the "OUTPUT 0-9" connector (Fig. 5-2).



Fig. 5-2 Fastening the Front Panel at the Connector

- Fasten the front panel at the top with the raised countersunk head screw M2.5x8 to the bracket attached previously.
- Fasten the front panel at the bottom and the front panel handle to the bracket attached previously using the Pozidrive flathead screw M2.5x16 (Fig. 5-3).



Fig. 5-3 Attaching the Upper and Lower Fastening Screws

• Finally press the identification plate into the extraction handle.

You have now mounted the front panel for a PB4350XXX module.

5.2 Mounting the CAN Transceivers

Note

The ES1651.1 Carrier Board is normally delivered with its CAN transceivers already assembled. The following description is purely for the sake of completeness.

Proceed as follows to mount the piggybacks with the CAN transceivers:

- Position the piggyback on the two female headers intended.
- Make sure the pins of the module match the corresponding contacts exactly.
- Press the module pins into the female headers by pressing left and right alternately (see arrows in Fig. 5-4).





Mounting the CAN Transceivers

• Then tighten the piggyback on the ES1651.1 Carrier Board with the M2.5x13 screw provided.

5.3 Mounting the I/O Modules

Proceed as follows to mount the I/O modules.

To mount distance pins on the ES1651.1 Carrier Board

- Make sure you have four distance pins at hand which have an internal thread on both sides.
- Get out four screws.
- Screw all four distance pins onto the ES1651.1 Carrier Board (distance pins on the component side, screws on the solder (dip) side, see Fig. 5-5)





- Insert the ribbon cable delivered with the corresponding I/O module into Slot 0.
- If you want to mount further I/O modules, insert the ribbon cable correspondingly into Slot 1, then Slot 2, Slot 3 etc.



Fig. 5-6 Inserting the Ribbon Cable To mount I/O modules

Note

If you only want to mount one I/O module, continue with "To mount the last I/O module" on page 32.

- Make sure you have four distance pins at hand which have an external thread on one side.
- Lie the I/O module on the distance pins you have just mounted on the Carrier Board.
- Tighten the I/O module with the distancepins (see Fig. 5-7 on page 32).
- Slot the connector of the relevant ribbon cable into the box header of the I/O module.



Fig. 5-7 Mounting the I/O Module

• Mount further I/O modules in the same way. The mounting of the last module is described in the following section.

To mount the last I/O module

• Mount the last I/O module as described above – it is tightened, however, with four screws (see Fig. 5-8 on page 33).



Fig. 5-8 Mounting the Last I/O Module

6 Pin Assignments and Display Elements

This section contains a description of the pin assignments of the connectors on the front panel and on the board itself and the meaning of the display elements on the front panel.

The position and name of the individual elemenets is shown in Fig. 4-1 on page 20.

These are:

- "CAN Ports CAN0 and CAN1 (CO0, CO1)" on page 34
- "Synchronization Bus and CAC Bus Connection "SYNC & CAC" (CO2)" on page 35
- "Connectors for CAN Transceiver Modules" on page 36
- "Box Headers for I/O Modules (CO7 CO10)" on page 37
- "LEDs" on page 39

6.1 CAN Ports CAN0 and CAN1 (CO0, CO1)

Socket - LEMO 8-pin. Type: Lemo EPC.1B.308.HLN



Fig. 6-1 CO0 ("CAN0") and CO1 ("CAN1") Connectors (View from the Plug-In Side)

The mating connector is of type Lemo FGC.1B.308.CLA052.

Pin	Assignment	Pin	Assignment
1	Wake	5	n.c.
2	CAN Low	6	CAN ground/-UBatt
3	CAN ground/-UBatt	7	CAN High
4	n.c.	8	+UBatt



6.2 Synchronization Bus and CAC Bus Connection "SYNC & CAC" (CO2)

Socket - Sub-D 9-pin.



Fig. 6-2 "SYNC & CAC" Socket (View from the Plug-In Side)

Pin	Signal	Direction	Function
1	SYNC0	Bi-directional	Synchronization line 0
2	SYNC1	Bi-directional	Synchronization line 1
3	SYNC2	Bi-directional	Synchronization line 2
4	SYNC3	Bi-directional	Synchronization line 3
5	Ground	-	VMEbus ground
6	CAC_SYNC	Bi-directional	Crankshaft angle clock: Synchronization signal for 0° CA
7	CAC_CLK	Bi-directional	Crankshaft angle clock: Crankshaft angle signal
8	CAC_DOR	Bi-directional	Crankshaft angle clock: Direction of rotation signal
9	Ground	-	VMEbus ground

Tab. 6-2"SYNC & CAC" Pin Assignment

6.3 Connectors for CAN Transceiver Modules





6.3.1 8-Pin Female Header (CO3, CO5)

Pin	Assignment
1	Housing ground
2	+3.3 V
3	/Wake
4	CAN_L
5	CAN_H
6	+UBatt
7	-UBatt/CAN ground
8	VMEbus ground

Fig. 6-4 CO3/CO5 Pin Assignment

Pin	Assignment	Pin	Assignment	
1	TxD	2	RxD	
3	HsON	4	HsTERM	
5	/FtStandby	6	FtEnable	
7	/FtError	8	MOSI	
9	MISO	10	SCLK	
11	/CSEL	12	USRO	
13	USR1	14	TPB_AV	
15	+5 V	16	VMEbus ground	

6.3.2 16-Pin Female Header (CO4, CO6)

Tab. 6-3 CO4/CO6 Pin Assignment

6.4 Box Headers for I/O Modules (CO7 - CO10)



Fig. 6-5 Box Headers for Connecting I/O Modules

Pin	Assignment	Pin	Assignment
1	/RESET	2	SOUT
3	SDIN	4	SCLK
5	/SCS0	6	/SCS1
7	TDO	8	TDI
9	TMS	10	ТСК
11	/IRQ	12	PROG_DONE
13	CAC_CLK	14	CAC_SYNC
15	CAC_DOR	16	SYNCO
17	SYNC1	18	SYNC2
19	SYNC3	20	PB_AV
21	GND	22	+5 V
23	+5 V	24	+3.3 V
25	+3.3 V	26	+2.5 V
27	GND	28	GND
29	AGND	30	AGND
31	+12 V	32	+12 V
33	-12 V	34	-12 V

Tab. 6-4 CO7 - CO10 Pin Assignment

6.5 ETAS-Internal Service Connection (CO11)

CO11 provides various access possibilities for ETAS-internal purposes such as e.g. RS232, Debug, JTAG, Boundary Scan.

6.6 Interface for Logic Analyser (CO12)

A further debug interface for ETAS-internal purposes.

6.7 LEDs

There are 6 LEDs on the front panel of the ES1651.1 Carrier Board, the meaning of which is described below.



Tab. 6-5Significance of the LEDs

7 Technical Data

This chapter contains the technical data of the ES1651.1 Carrier Board.

Number of slots	4
Supported types of I/O modules	PB1651XXX and PB4350XXX
Configuration of the I/O mod- ules	PB1651XXX and PB4350XXX, mixed
Synchronization of I/O modules	Yes
Number of synchronization signals	4
Sources of the synchronization signals	- I/O module - ES4350.1 processor/FPGA - ES4300 backplane

Synchronization Bus: Outputs

Logic level	TTL (5 V)
Maximum output current	6 mA
Cutoff frequency f _{max}	1.2 MHz
Overvoltage protection	-14 V +19 V

Synchronization Bus: Inputs

Logic level	TTL (5 V)
Input impedance	> 200 kΩ
Cutoff frequency f _{max}	1.2 MHz
Overvoltage protection	-14 V +19 V

CAC Bus: Output (All CAC Bus Signals)

Logic level	TTL (5 V)
Maximum output current	6 mA
Cutoff frequency f _{max}	1.2 MHz
Overvoltage protection	-14 V +19 V

CAC Bus: Input (CAC-SYNC and CAC_CLK Signal)

Supported CAC signal forms	 Combined CAC synchronization and clock signal in acc. with Fig. 2-5 on page 15 CAC bus signals in acc. with Fig. 2-4 on page 14
Input impedance	> 200 kΩ
Cutoff frequency f _{max}	1.2 MHz
Overvoltage protection	-14 V +19 V

CAC Bus: Input (CAC-DOR Signal)

Logic level	TTL (5 V)
Input impedance	> 200 kΩ
Cutoff frequency f _{max}	1.2 MHz
Overvoltage protection	-14 V +19 V

Power Supply

Current consumption*	1 A @ +5 V DC	
	0.1 A @ +12 V DC	
	0.1 A @ -12 V DC	

* Underlying conditions: No I/O moduls assembled – CAN transceiver moduls assembled and CAN in operation.

Environmental Conditions

Operating temperature	5 °C to 35 °C (5.00 °C to 35.00 °C)
Relative humidity	0 to 95% (non-condensing)

Physical Dimensions

Printed circuit board (L x W)	145 mm x 100 mm
Front panel	Height: 3 U
	Width: 4 HP

8 ETAS Contact Addresses

ETAS HQ		
ETAS GmbH		
Borsigstraße 24	Phone:	+49 711 3423-0
70469 Stuttgart	Fax:	+49 711 3423-2106
Germany	WWW:	www.etas.com

ETAS Subsidiaries and Technical Support

For details of your local sales office as well as your local technical support team and product hotlines, take a look at the ETAS website:

ETAS subsidiaries	WWW:	www.etas.com/en/contact.php
ETAS technical support	WWW:	www.etas.com/en/hotlines.php

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