ES1650.1 Piggyback Carrier Board

User's Guide

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Contents

1 Introduction

This section contains information about the basic features and applications of the ES1650.1 Piggyback Carrier Board. A block diagram shows the schematic layout of the board.

note

Some components of the board may be damaged or destroyed by electrostatic discharges. Please keep the board in its storage package until it is installed. The board should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

note

The components, connectors, and printed lines of the board may carry dangerous high voltages.
These voltages may even exist when the board is not installed in the VME system or when the VME system is powered off. Make sure that the board is protected against contact during its operation.
Disconnect all connections to the ES1650.1 Piggyback Carrier Board before removing the board from the VME system.

1.1 Features

The ES1650.1 Piggyback Carrier Board is used in VMEbus systems as a carrier board for piggybacks. The board can hold two piggybacks. There are piggybacks for a variety of tasks, such as digital and analog input and output modules as well as relay modules with switching capability.

The piggybacks are connected to the carrier board via connector sockets. The ports of the piggybacks are provided on the front panel via a 50-pin connector. The signal pins of the front panel connector are electrically isolated from the VMEbus.

The carrier board has a VMEbus slave interface - the board can be configured for different address ranges using jumpers.

The following figure shows the front panel of the carrier board and the position of the front panel connectors.

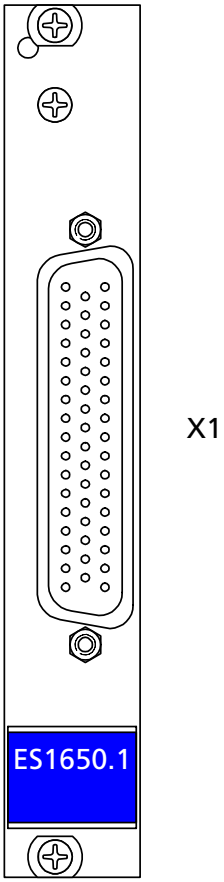


Fig. 1-1 ES1650.1 Piggyback Carrier Board Front Panel

1.2 Block Diagram

The block diagram illustrates the schematic layout of the board.

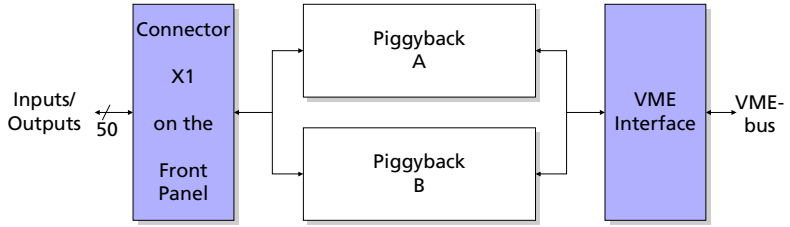


Fig. 1-2 ES1650.1 Block Diagram

The 50-pin connector is visible on the left side of the front panel. It is wired to the two piggybacks. The VMEbus interface is located on the extreme right. This interface converts the signals of the VMEbus into data, address, and control signals for the piggybacks.

The pins of the front panel connector are electrically isolated from the VMEbus.

1.3 ES1650.1 Hardware

This section provides a detailed overview of the features of the ES1650.1 Piggyback Carrier Board. You will find information on the following subjects:

- carrier for piggybacks
- external local reset

1.3.1 Carrier for Piggybacks

The ES1650.1 Piggyback Carrier Board is used in VMEbus systems as a carrier for piggybacks. Piggybacks are available for various analog and digital signal input and output tasks.

On the front panel, the board provides a 50-pin connector for the inputs and outputs of the piggybacks. This connector is electrically isolated from the VMEbus.

On the VMEbus side, the carrier board is responsible for address selection and for buffering the data, address, and control lines of the VMEbus. The ES1650.1 Piggyback Carrier Board is equipped with a slave interface with 24 address lines and 16 data lines. Different size address ranges within the address space of the VMEbus can be assigned to the piggybacks. The base address and the size of the address range are configured by jumpers.

1.3.2 External Local Reset

The front panel connector provides two pins that can be used to trigger a local reset of the piggybacks. If you intend to use this function, these two pins need to be connected to a relay.

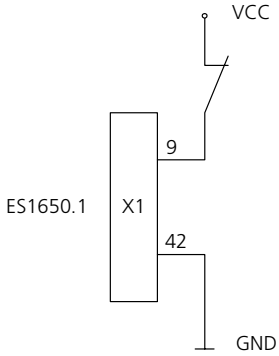


Fig. 1-3 Relay for the Local Reset

The local reset is triggered when the connection between the two pins is interrupted. The pins, however, have to be supplied with 5 V < VCC < 48 V. The reset only affects the piggybacks and *not* the VMEbus.

note

If pins 9 and 42 of the front-facing connector X1 remain disconnected and the external reset was triggered by jumper B20, there can be a sporadic reset of the piggybacks.
Connect pins 1 and 2 of jumper B20 if you are not using the external reset and leave pins 9 and 42 disconnected.

If you use more than one ES1650.1 Piggyback Carrier Board in a system and wish to use a common local reset for all boards, you can connect the corresponding pins of the boards in series with the relays.

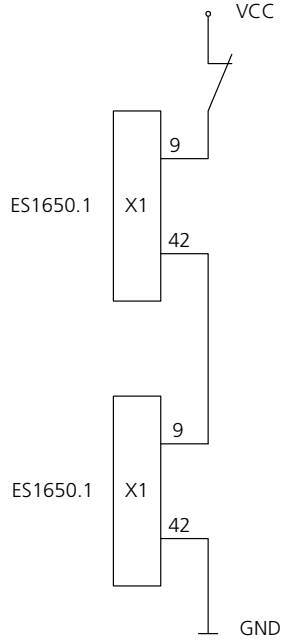


Fig. 1-4 Local Reset for Several Carrier Boards

A jumper can be used to disable the function of the two front panel pins so that an external local reset cannot be triggered.

1.4 Hardware Configuration

This section contains information on configuring the jumpers of the ES1650.1 Piggyback Carrier Board. The jumpers are used to configure the following settings:

- VMEbus base address and size of address range
- address modifier
- local reset

The figure shows the position of the jumpers and connector sockets for the piggybacks.

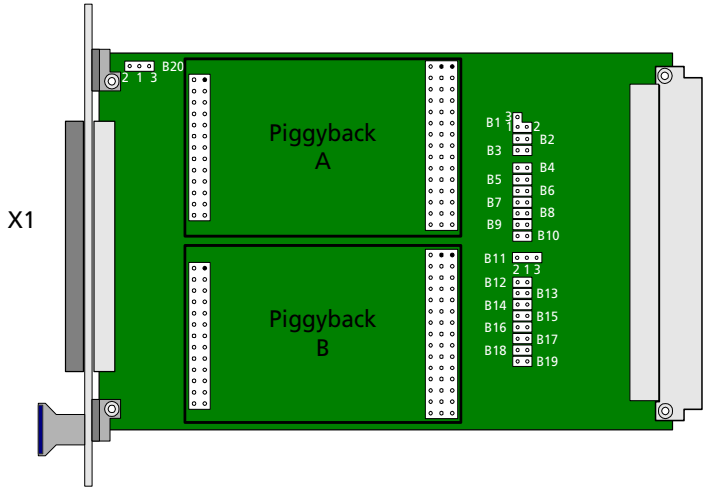


Fig. 1-5 ES1650.1 Position of the Jumpers (Component Side)

1.4.1 VMEbus Base Address

The base address of the ES1650.1 Piggyback Carrier Board is selected by the five jumpers B2, B12, B13, B14, and B15.

note

*Make sure that the address range of the ES4120 board does **not** overlap address ranges of other boards in your system.*

If you chose an address block size of 256 bytes, you can use 32 different address settings in the range $FE0400 to $FEFC00. For an address block size of 8 KBytes, jumpers B14 and B15 are ignored. This provides only eight address settings. The default base address of the board is $FE0400.

note

A closed jumper means logical "0"; an open jumper means logical "1".

Jumper	Address	Default Setting
B2	A15	Closed
B12	A14	Closed
B13	A13	Closed
B14	A12	Closed
B15	A11	Closed

Tab. 1-1 Assignment of Jumper and Address Line

The following table provides you with an overview of the configuration of jumpers B2, and B12 to B16 for the base addresses of the 256-byte blocks. "o" stands for an open jumper; "c" for a closed jumper.

Address Range	B2	B12	B13	B14	B15	B16
0xFE0400 - 0xFE04FF	c	c	c	c	c	o
0xFE0C00 - 0xFE0CFF	c	c	c	c	o	o
0xFE1400 - 0xFE14FF	c	c	c	o	c	o
0xFE1C00 - 0xFE1CFF	c	c	c	o	o	o
0xFE2400 - 0xFE24FF	c	c	o	c	c	o
0xFE2C00 - 0xFE2CFF	c	c	o	c	o	o
0xFE3400 - 0xFE34FF	c	c	o	o	c	o
0xFE3C00 - 0xFE3CFF	c	c	o	o	o	o
0xFE4400 - 0xFE44FF	c	o	c	c	c	o
0xFE4C00 - 0xFE4CFF	c	o	c	c	o	o
0xFE5400 - 0xFE54FF	c	o	c	o	c	o
0xFE5C00 - 0xFE5CFF	c	o	c	o	o	o
0xFE6400 - 0xFE64FF	c	o	o	c	c	o
0xFE6C00 - 0xFE6CFF	c	o	o	c	o	o
0xFE7400 - 0xFE74FF	c	o	o	o	c	o

Tab. 1-2 Base Address and Jumper Configuration

Address Range	B2	B12	B13	B14	B15	B16
0xFE7C00 - 0xFE7CFF	c	o	o	o	o	o
0xFE8400 - 0xFE84FF	o	c	c	c	c	o
0xFE8C00 - 0xFE8CFF	o	c	c	c	o	o
0xFE9400 - 0xFE94FF	o	c	c	o	c	o
0xFE9C00 - 0xFE9CFF	o	c	c	o	o	o
0xFEA400 - 0xFEA4FF	o	c	o	c	c	o
0xFEAC00 - 0xFEACFF	o	c	o	c	o	o
0xFEB400 - 0xFEB4FF	o	c	o	o	c	o
0xFEBC00 - 0xFEBCFF	o	c	o	o	o	o
0xFEC400 - 0xFEC4FF	o	o	c	c	c	o
0xFECC00 - 0xFECCFF	o	o	c	c	o	o
0xFED400 - 0xFED4FF	o	o	c	o	c	o
0xFEDC00 - 0xFEDCFF	o	o	c	o	o	o
0xFEE400 - 0xFEE4FF	o	o	o	c	c	o
0xFEEC00 - 0xFEECFF	o	o	o	c	o	o
0xFEF400 - 0xFEF4FF	o	o	o	o	c	o
0xFEFC00 - 0xFEFCFF	o	o	o	o	o	o

Tab. 1-2 Base Address and Jumper Configuration (cont'd)

The following table shows you the configuration of jumpers B2, and B12 to B16 for the base addresses of the 8-KByte blocks. "o" stands for an open jumper; "c" for a closed jumper. Jumpers marked with "x" are not evaluated.

Address Range	B2	B12	B13	B14	B15	B16
0xFE0000 - 0xFE1FFF	c	c	c	x	x	c
0xFE2000 - 0xFE3FFF	c	c	o	x	x	c
0xFE4000 - 0xFE5FFF	c	o	c	x	x	c
0xFE6000 - 0xFE7FFF	c	o	o	x	x	c
0xFE8000 - 0xFE9FFF	o	c	c	x	x	c
0xFEA000 - 0xFEBFFF	o	c	o	x	x	c
0xFEC000 - 0xFEDFFF	o	o	c	x	x	c
0xFEE000 - 0xFEFFFF	o	o	o	x	x	c

Tab. 1-3 Base Address and Jumper Configuration

1.4.2 Size of the Address Range

The size of the address range occupied by the ES1650.1 Piggyback Carrier Board in your system is selected by jumper B16. You can choose between the sizes 265 bytes and 8 KBytes. The size that needs to be set depends on the piggybacks used.

Jumper	Open	Closed
B16	256-byte (default setting)	8-KByte

1.4.3 Address Modifier

The B3 jumper determines the address modifier. You can choose between the access types "Short Access" (29/2D) and "Standard Access" (39/3D/00)

Jumper	Open	Closed
B3	Standard Access (default setting)	Short Access

1.4.4 Local Reset

You can trigger a local reset of the piggybacks by using an external connector pin on the front panel. Use jumper B20 to specify whether this external connector pin is to be evaluated.

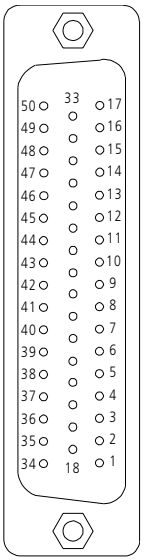
Jumper	Source of the Interrupt Vector
B20 open	Setting *not* allowed
B20 pins 1-2 closed	External local reset *not* possible
B20 pins 1-3 closed	External local reset possible

note

*Either pins 1-2 or 1-3 of the B20 jumper **must** be connected. If both jumpers are open, the local reset may be triggered by accident.*

1.5 Pin Assignment

This section describes the pin assignments of the ES1650.1 Piggyback Carrier Board.



X1

Fig. 1-6 ES1650.1 Pin Assignments on the Front Panel

In the table below, the letter in the "Piggyback Pin" column indicates the position of the piggyback. "A" designates the upper, "B" the lower piggyback. The number following the letter indicates the pin number of the frontal connector plug for the particular piggyback. The tables with the pin assignments of the piggybacks can be found in the relevant documentation for the individual piggybacks.

X1 Pin	Piggyback Pin	X1 Pin	Piggyback Pin
1	B24	26	A24
2	B21	27	A21
3	B18	28	A18
4	B15	29	A15
5	B12	30	A12
6	B9	31	A9
7	B6	32	A6

Tab. 1-4 ES1650.1 Pin Assignment

X1 Pin	Piggyback Pin	X1 Pin	Piggyback Pin
8	B3	33	A3
9	Ext. reset supply voltage	34	B23
10	A23	35	B20
11	A20	36	B17
12	A17	37	B14
13	A14	38	B11
14	A11	39	B8
15	A8	40	B5
16	A5	41	B25, B26
17	A25, A26	42	Ext. reset GND
18	B22	43	A22
19	B19	44	A19
20	B16	45	A16
21	B13	46	A13
22	B10	47	A10
23	B7	48	A7
24	B4	49	A4
25	B1, B2	50	A1, A2

Tab. 1-4 ES1650.1 Pin Assignment

note

The components as well as the component and solder sides of the ES1650.1 Piggyback Carrier Board and its piggybacks may carry dangerous high voltages. These dangerous voltages may even exist if the VMEbus system is powered off or the ES1650.1 Piggyback Carrier Board has been removed.
Be sure to disconnect the front panel connector of the ES1650.1 Piggyback Carrier Board before removing the board or touching the removed board!

1.6 Technical Data

This section contains the technical data of the ES1650.1 Piggyback Carrier Board in tabular form.

VMEbus

Type	Slave interface
Address and data lines	24-bit address and 16-bit data, or 16-bit address and 16-bit data
Base address	$FE0400 to $FEFC00 selected by jumpers
Address modifier	Standard or short supervisor/user data

Power Supply

Basic board	+5 V DC, ±5 %, max. 140 mA without piggybacks

Environmental Conditions

Ambient temperature during operation	0 °C to +70 °C
Storage temperature	-55 °C to +85 °C
Relative humidity	5 to 95 %, no condensation

Connectors

Backplane	96-pin DIN 41612 C
Front panel	50-pin Submin-D socket strip
Piggybacks	One 26-pin connector at the front and one 45-pin connector at the VMEbus side for each piggyback

Circuit board	100 x 160 mm²
Front panel	Height: 3 U Width: 4 HP (20.3 mm)

2 PB1650DAC1.1 D/A Piggyback (4 Channels)

This section contains information about the basic features and applications of the PB1650DAC1.1 D/A piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

2.1 Features

The PB1650DAC1.1 piggyback is used to generate analog output signals in VMEbus systems in conjunction with the ES1650.1 Piggyback Carrier Board. The module has the following features:

- digital/analog conversion with 12-bit resolution
- four optional unipolar or bipolar output channels
- its own control interface and ID byte
- separately programmable reference voltage for each channel
- analog output channels electrically isolated from the VMEbus system

2.2 Applications

The PB1650DAC1.1 is used in conjunction with the ES1650.1 Piggyback Carrier Board in VMEbus systems to generate earth-free analog output voltages.

2.3 Block Diagram

The block diagram below illustrates the working principle of the piggyback.

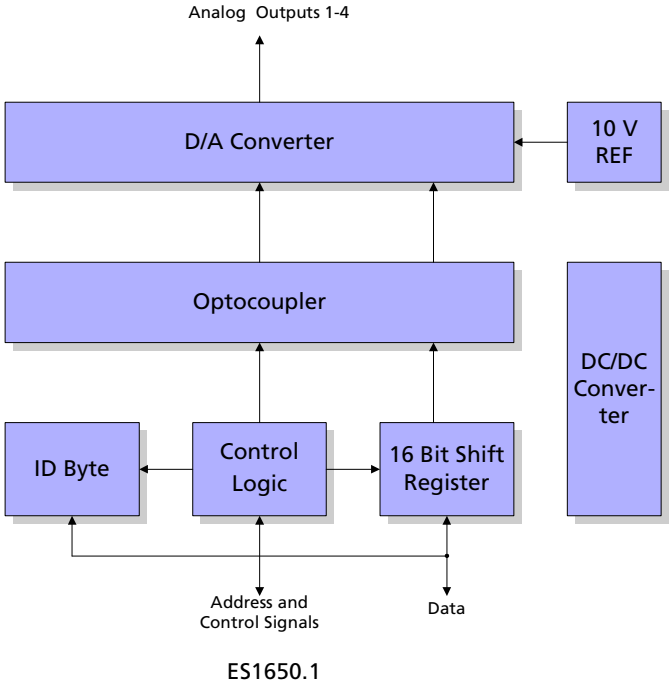


Fig. 2-1 PB1650DAC1.1 Block Diagram

At the bottom left of the block diagram, you see the control interface of the piggyback that on the one hand is connected with the VMEbus and passes data and the clock signal to the digital/analog converter through an optocoupler. Signals are transferred between the VMEbus and the piggyback via the 16-bit shift register at the bottom right of the diagram. The D/A converter at the top of the diagram has eight output channels: four output channels are used to generate the reference voltages for a channel and the other four are used to generate the required analog voltage. The outputs can be used in unipolar or bipolar mode.

2.4 PB1650DAC1.1 Hardware

This section gives you a detailed overview of the features of the PB1650DAC1.1 piggyback. You will find information on the following subjects:

- signal conditioning
- output voltage range
- digital/analog converter
- control interface
- size of the address range

The following figure shows the position of the components of the PB1650DAC1.1 piggyback.

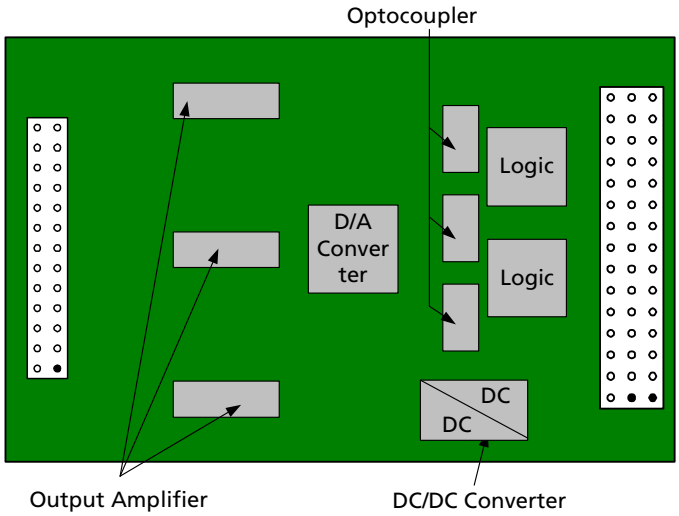


Fig. 2-2 Component Side of the PB1650DAC1.1

2.4.1 Signal Conditioning

The piggyback has four D/A output channels that are electrically isolated from the VMEbus system. Unipolar or bipolar conversion can be selected by solder straps. The reference voltage can be set for each channel separately.

The figure shows channel A as an example of how the output stage is realized.

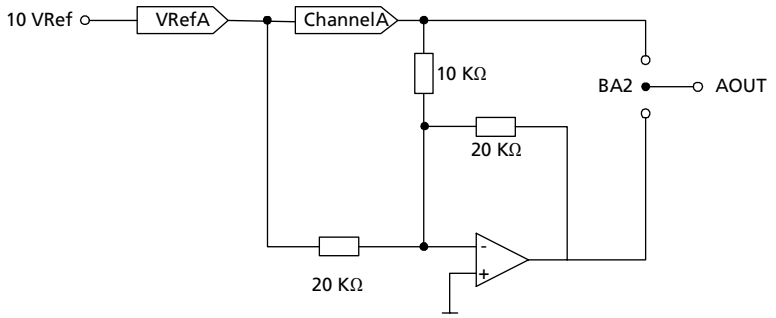


Fig. 2-3 Output Circuit of the D/A Converters

The voltages of the reference output A and channel A are each generated by an output of the A/D converter.

2.4.2 Output Voltage Range

In unipolar mode, the output voltage of each output is 0 V to +10 V.

In bipolar mode, the voltage is -10 V to +10 V.

The unipolar or bipolar mode can be set separately for each output.

2.4.3 Digital/Analog Converter

The digital/analog converter features a 12-bit resolution while the serial data transfer time is 4 µs per data word. The D/A converter is electrically isolated from the voltage supply of the VMEbus system.

2.4.4 Control Interface

The control interface of the PB1650DAC piggyback consists of two shift registers and PAL logic. It controls the 16-bit parallel/serial conversion and the data flow to the converter.

The interface also generates clock signals and the status register enabling access to the EOS (end of shift) and EOP (end of programming) signals.

Additionally, the control interface generates the "$EA" ID byte for the PB1650DAC1.1 piggyback. The ID byte can be used to read the equipment of the carrier board using a software program.

2.4.5 Size of the Address Range

The size of the address range occupied by the PB1650DAC1.1 in your system is 256 bytes.

The B16 jumper on the ES1650.1 carrier board has to be open for this address range size.

2.5 Configuration

The PB1650DAC1.1 piggyback has four groups of solder straps on the solder side, one group for each output channel. They are used to select the unipolar or bipolar mode for the output voltage.

The position of each solder strap is shown in the following figure.

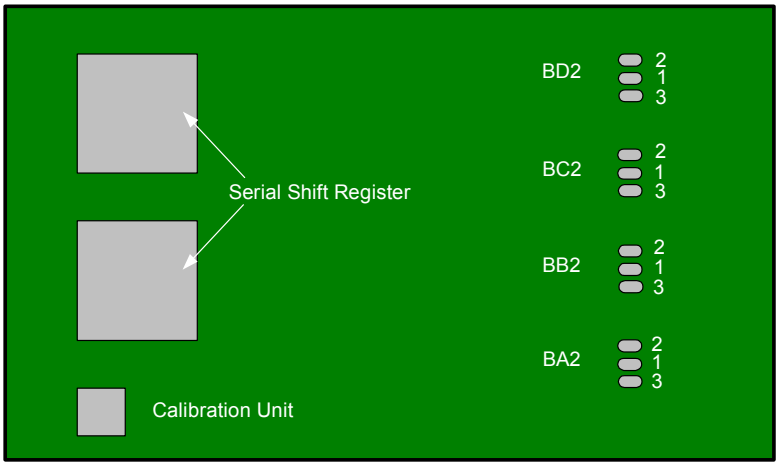


Fig. 2-4 Solder Side of the PB1650DAC1.1

The table provides you with an overview of the available functions and the corresponding position of the solder straps.

Channel	Solder Strap	Position	Function
A	BA2	1, 2 closed 1, 3 closed	Unipolar mode Bipolar mode (default setting: ds)
B	BB2	1, 2 closed 1, 3 closed	Unipolar mode Bipolar mode (ds)
C	BC2	1, 2 closed 1, 3 closed	Unipolar mode Bipolar mode (ds)
D	BD2	1, 2 closed 1, 3 closed	Unipolar mode Bipolar mode (ds)

Tab. 2-1 Output voltage range of the PB1650DAC1.1

2.6 Pin Assignment

The pin assignment of the X1 front connector of the ES1650.1 Piggyback Carrier Board depends on whether the piggyback is mounted in position A (top) or in position B (bottom).

The following two tables explain each of the two possible pin layouts.

The first letter of the signal name indicates one of the four channels A, B, C or D. "OUT" designates the signal pin of the channel and "GND" the associated ground pin.

Signal	X1 Pin	Signal	X1 Pin
AOUT	14	AGND	30
		AGND	47
BOUT	29	BGND	13
		BGND	45
COUT	44	CGND	11
		CGND	28
DOUT	10	DGND	26
		DGND	43
Ext. reset supply voltage	9	Ext. reset GND	42
Open	12	Open	32
Open	15	Open	33
Open	16	Open	46
Open	17	Open	48
Open	27	Open	49
Open	31	Open	50

Tab. 2-2 Pin Assignment of the PB1650DAC1.1 - Piggyback in Position A

Signal	X1 Pin	Signal	X1 Pin
AOUT	38	AGND	5
		AGND	22
BOUT	4	BGND	20
		BGND	37
COUT	19	CGND	3

Tab. 2-3 Pin Assignment of the PB1650DAC1.1 - Piggyback in Position B

Signal	X1 Pin	Signal	X1 Pin
		CGND	35
DOUT	34	DGND	1
		DGND	18
Open	2	Open	24
Open	6	Open	25
Open	7	Open	36
Open	8	Open	39
Open	21	Open	40
Open	23	Open	41

Tab. 2-3 Pin Assignment of the PB1650DAC1.1 - Piggyback in Position B

2.7 Technical Data

This sections contains the technical data of the PB1650DAC1.1 digital/analog converter piggyback in tabular form.

D/A Converter

Resolution	12-bit
Serial data transfer time	4 µs per data word
Rise time	0.4 V per µsec
Linearity error	±0.75 LSB
Differential linearity	±0.9 LSB
Type	AD 7568 from Analog Devices

Analog Output

Output voltage in unipolar mode	0 V to +10 V for each output selected by solder straps
Output voltage in bipolar mode	-10 V to +10 V for each output selected by solder straps
Output current	Max. 2 mA per channel

Power Supply

Piggyback	+5 V DC, ±5 %, max. 290 mA

Environmental Conditions

Ambient temperature during operation	0 °C to +70 °C
Storage temperature	-55 °C to +85 °C
Relative humidity	5 to 95 %, no condensation

3 PB1650DIO1.1 Digital I/O Piggyback (8/8 Channels)

This section contains information about the basic features and applications of the PB1650DIO1.1 digital I/O piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

note

The components, connectors, a nd printed lines of the piggyback may carry dangerous high voltages.
These voltages may even exist when the piggyback is not installed in the VME system or when the VME system is powered off.
Make sure that the piggyback is protected against contact during its operation.
Disconnect all connections to the ES1650.1 Piggyback Carrier Board before removing the board from the VME system.

3.1 Features

The PB1650DIO1.1 piggyback is intended for digital input and output of switching states via eight input and eight output ports that are electrically isolated.

The piggyback provides the following features:

- eight parallel, electrically isolated digital input channels (max. 80 V DC)
- eight parallel, electrically isolated digital output channels (max. 500 mA)
- its own ID byte

3.2 Applications

The PB1650DIO1.1 piggyback is used in conjunction with the ES1650.1 Piggyback Carrier Board in VMEbus systems for capturing and generating binary switching signals.

Examples of applications are:

- acquisition of output states of the ECU (energizing solenoids, reversing light relays)
- switch simulation (hand brake switch)

3.3 Block Diagram

The block diagram below illustrates the working principle of the PB1650DIO1.1 piggyback.

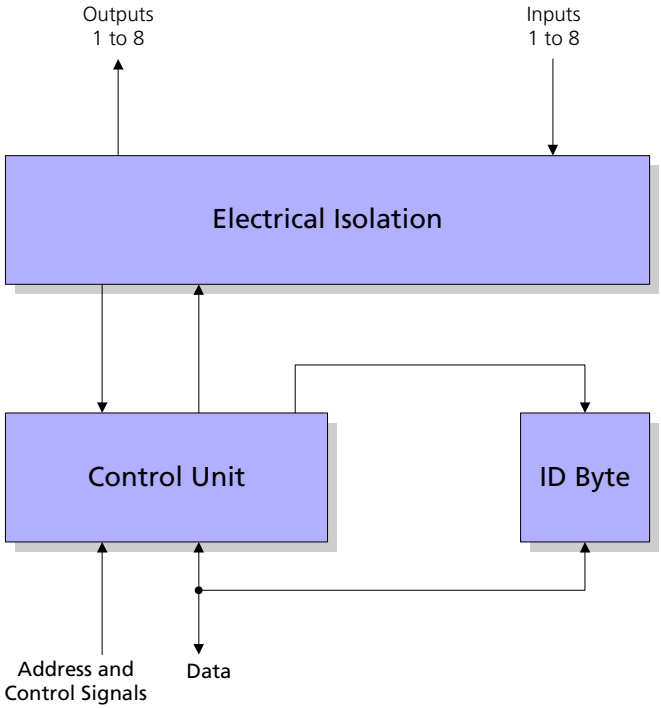


Fig. 3-1 PB1650DIO1.1 Block Diagram

In the top center, you can see the electrical isolation separating the 16 input and output channels from each other and from the VMEbus system. Below it, you find the module-internal control unit. This controls the digital inputs and outputs and generates the ID byte of the piggyback.

3.4 PB1650DIO1.1 Hardware

This section gives you a detailed overview of the features of the PB1650DIO1.1 piggyback. You will find information on the following subjects:

- inputs
- outputs
- power ON state
- control interface
- size of the address range

The following figure shows the position of the components on the piggyback.

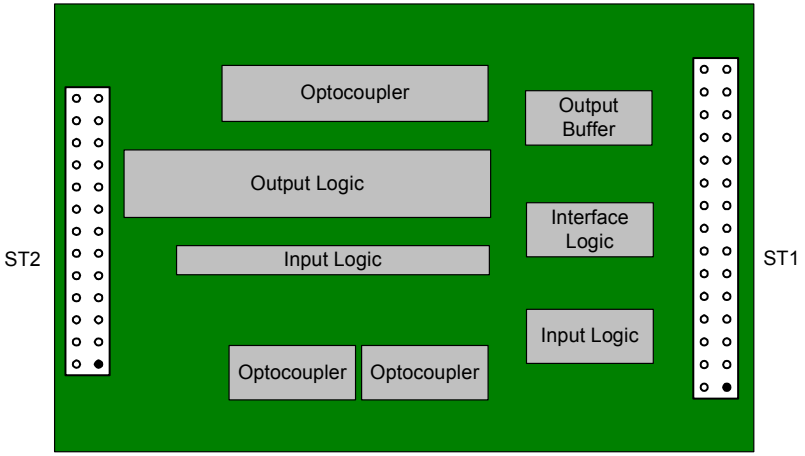


Fig. 3-2 Component Side of the PB1650DIO1.1

3.4.1 Inputs

The input area consists of one opto-isolated input with current limitation and one input buffer to the ES1650.1 interface. There are eight parallel input channels in groups of two channels sharing one common ground per group. The input voltage range is a max. of 80 V DC.

The input current is limited to 5 mA. The input circuit does not invert.

Input levels <5 V are interpreted as a logical 0, and input levels >10 V as a logical 1. In the range from 5 V to 10 V, the switching state is undefined.

The channels 1 and 2, 3 and 4, 5 and 6, 7 and 8 each share a common ground port.

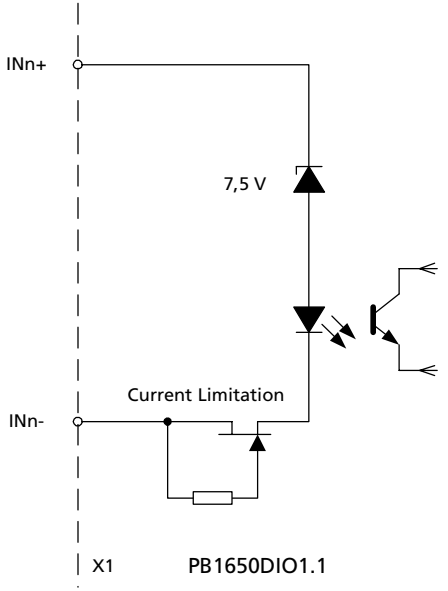


Fig. 3-3 Input Circuit of the PB1650DIO1.1

3.4.2 Outputs

The output driver consists of a bipolar transistor switch, an optocoupler, and a safety diode. There are eight parallel, electrically isolated output channels in groups of two channels sharing one common ground per group.

The maximum output current per channel may not exceed 500 mA. The output voltage must be between +5 V and +80 V. Each channel can be programmed individually.

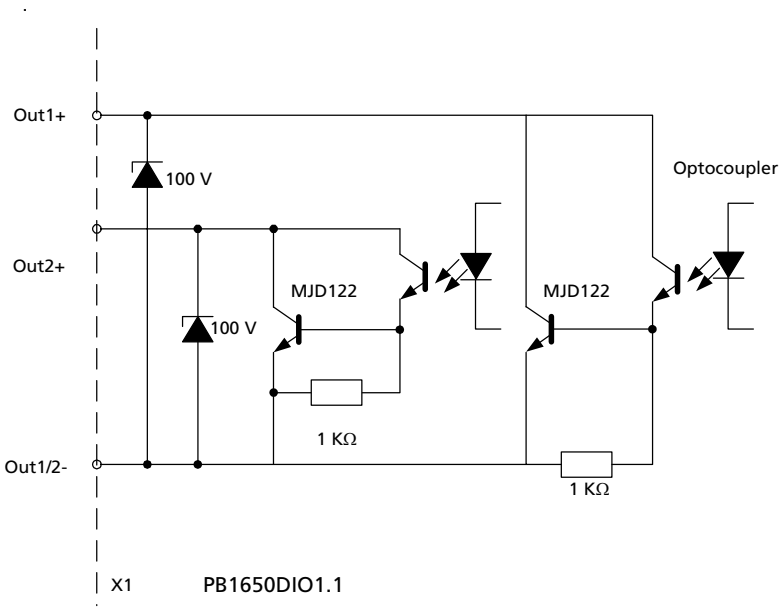


Fig. 3-4 Output Circuit of the PB1650DIO1.1

3.4.3 Power ON State

The output drivers are disabled in the power ON state and after a local reset. This means there is *no* output current.

The outputs are also disabled when the power supply of the VME system is off.

3.4.4 Control Interface

The control interface generates an ID byte for the piggyback.

The ID byte for the PB1650DIO1.1 piggyback is "$EF". The ID byte can be used to detect the equipment of the carrier board using a software program.

3.4.5 Size of the Address Range

The size of the address range occupied by the PB1650DIO1.1 in your system is 256 bytes.

The B16 jumper on the ES1650.1 Piggyback Carrier Board has to be open for this address range size.

3.5 Configuration

The PB1650DIO1.1 piggyback has *no* jumpers or solder straps that need to be configured.

3.6 Pin Assignment

The pin assignment of the ES1650.1 Piggyback Carrier Board depends on whether the piggyback is mounted in position A (top) or in position B (bottom).

The pin assignment for each position of the piggyback is shown in a table.

"IN" means input channel, and "OUT" stands for output channel. The numbers indicate the channel number. "+" indicates the signal output of the channel; "-" the ground port of the channel. Note that every two channels share a common ground.

Signal	X1 Pin	Signal	X1 Pin
OUT1+	17	IN1+	50
OUT2+	49	IN2+	33
OUT3+	15	IN3+	48
OUT4+	47	IN4+	31
OUT5+	13	IN5+	46
OUT6+	45	IN6+	29
OUT7+	11	IN7+	44
OUT8+	43	IN8+	27
OUT1/2-	32	IN1/2-	16
OUT3/4-	30	IN3/4-	14
OUT5/6-	28	IN5/6-	12
OUT7/8-	26	IN7/8-	10
Ext. reset supply voltage	9	Ext. reset GND	42

Tab. 3-1 Pin Assignment of the PB1650DIO1.1 - Piggyback in Position A (Top)

Signal	X1 Pin	Signal	X1 Pin
OUT1+	41	IN1+	25
OUT2+	24	IN2+	8
OUT3+	39	IN3+	23
OUT4+	22	IN4+	6
OUT5+	37	IN5+	21
OUT6+	20	IN6+	4
OUT7+	35	IN7+	19
OUT8+	18	IN8+	2
OUT5/6-	3	IN1/2-	40
OUT3/4-	5	IN3/4-	38
OUT1/2-	7	IN5/6-	36
OUT7/8-	1	IN7/8-	34

Tab. 3-2 Pin Assignment of the PB1650DIO1.1 - Piggyback in Position B (Bottom)

3.7 Technical Data

This section contains the technical data of the PB1650DIO1.1 piggyback in tabular form.

Digital Inputs

Input channels	Eight, opto-isolated, every two channels having one common ground
Input voltage	12 to 80 V DC
Switching level	<5 V = low >10 V = high
Input current	5 mA across the entire input voltage range

Digital Outputs

Output channels	Eight, opto-isolated, every two channels having one common ground
Output voltage	0 to 80 V DC
Supply voltage for external pull-up resistance	5 to 80 V DC
Output current	500 mA max.

Channel Properties

Input frequency	6.5 kHz max.
Isolation voltage	2500 V RMS between input and digital ground of VMEbus 100 V DC between inputs

Environmental Conditions

Ambient temperature during operation	0 to +70 °C
Storage temperature	-55 to +85 °C
Relative humidity	0 to 95% (no condensation)

Physical Dimensions

Length	100 mm
Width	48 mm
Depth	12 mm

4 PB1650DIO2.1 Digital I/O Piggyback (10/10 Channels)

This section contains information about the basic features and applications of the PB1650DIO2.1 digital I/O piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

4.1 Features

The PB1650DIO2.1 piggyback is used for the digital input and output of switching states via eight input and eight output ports which are dc decoupled.

The piggyback provides the following features:

- eight parallel, dc decoupled, digital input channels
- eight parallel, dc decoupled, digital output channels
- four parallel, dc decoupled, control lines
- its own ID byte

4.2 Applications

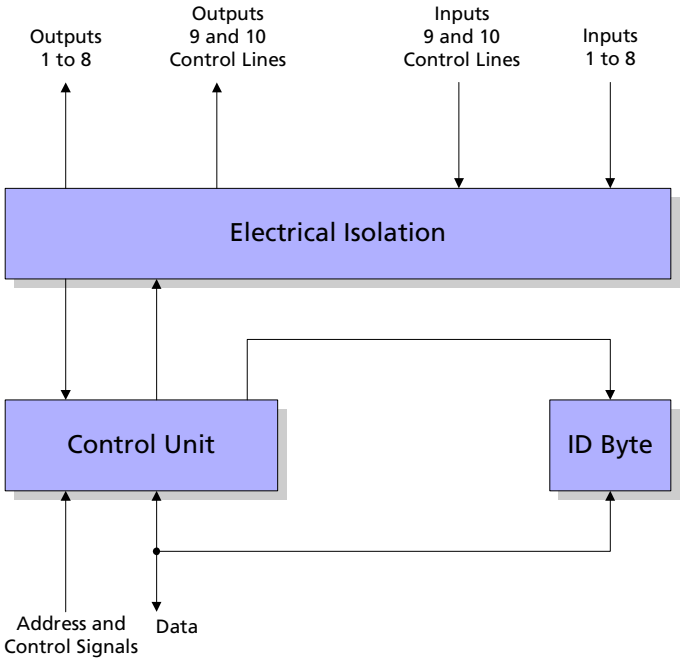
The PB1650DIO2.1 piggyback is used in conjunction with the ES1650.1 Piggyback Carrier Board in VMEbus systems for capturing and generating binary switching signals with TTL signal levels.

Examples of applications are:

- acquisition of switching outputs of the ECU (energizing solenoids, reversing light relays)
- switch simulation

4.3 Block Diagram

The block diagram below illustrates the working principle of the PB1650DIO2.1 piggyback.



ES1650.1

Fig. 4-1 PB1650DIO2.1 Block Diagram

In the top center, you can see the dc decoupling electrically separating the 16 input and output channels and the four control lines from the VMEbus system. Below it, you find the module-internal control unit. This controls the digital inputs and outputs and generates the ID byte of the piggyback.

4.4 PB1650DIO2.1 Hardware

This section gives you a detailed overview of the features of the PB1650DIO2.1 piggyback. You will find information on the following subjects:

- inputs
- outputs
- power ON state
- control interface
- size of the address range

The following figure shows the position of the components on the piggyback.

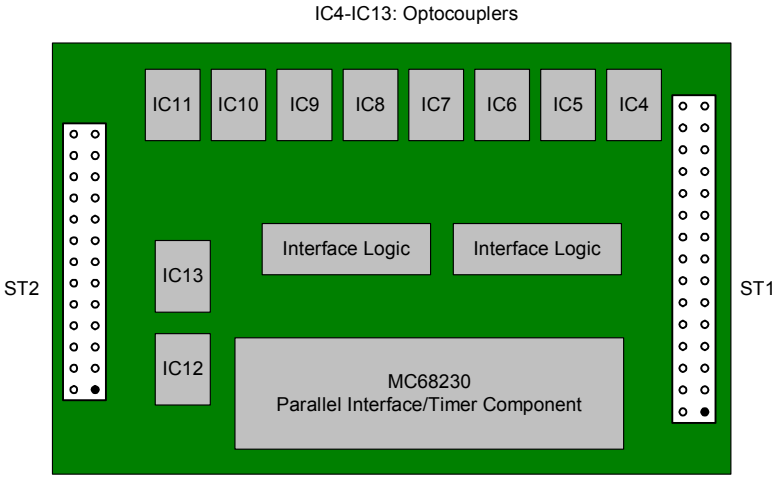


Fig. 4-2 Component Side of the PB1650DIO2.1

4.4.1 Inputs

The input area consists of one dc decoupled input and one input buffer to the ES1650.1 interface. There are eight parallel input channels and two parallel control lines. The two control lines, H1E and H3E, can either be configured as inputs or as control lines. The input voltage range is 0 to 5 V DC.

The following figure shows the allocation of an input channel.

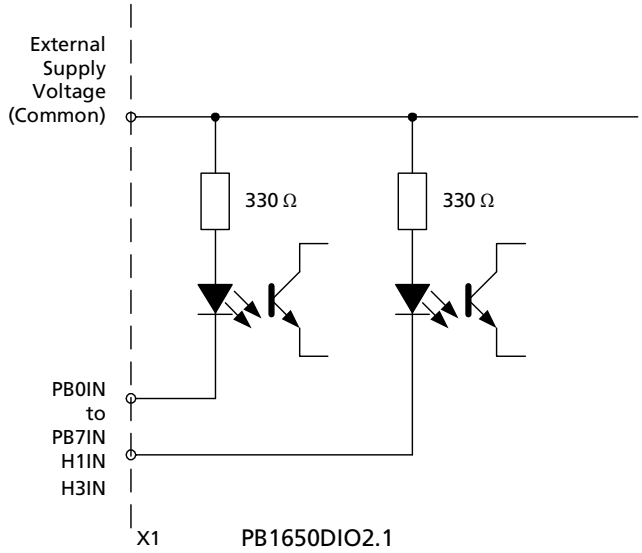


Fig. 4-3 Input Circuit of the PB1650DIO2.1

The input current must not exceed 10 mA. The input circuit does not invert.

Input levels <1.5 V are interpreted as a logical 0 (low), and input levels >3.0 V as a logical 1 (high). The switching state is undefined in the range 1.5 V to 3.0 V.

4.4.2 Outputs

The output drivers consist of a bipolar transistor switch and an optocoupler. There are eight parallel, dc decoupled output channels and two parallel control lines, H2E and H4E, which can be configured as outputs.

The following figure shows the allocation of an output channel.

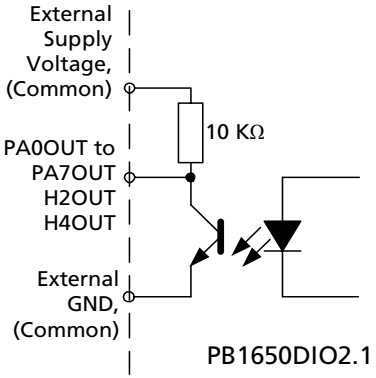


Fig. 4-4 Output Circuit of the PB1650DIO2.1

The maximum output current per channel must not exceed 10 mA. The outputs have a pull-up resistance of 10 kΩ.

All output and input channels have a common ground and supply voltage (VCC) which has to be applied from outside.

4.4.3 Power ON State

The output drivers are disabled in the power ON state and after a local reset. This means there is *no* output current.

The outputs are also disabled when the power supply of the VMEbus system is off.

4.4.4 Control Interface

The control interface generates an ID byte for the piggyback.

The ID byte for the PB1560DIO2.1 piggyback is "$F2". The ID byte can be used to detect the equipment of the carrier board using a software program.

4.4.5 Size of the Address Range

The size of the address range occupied by the PB1650DIO2.1 in your system is 256 bytes.

The B16 jumper on the ES1650.1 Piggyback Carrier Board has to be open for this address range size.

4.5 Configuration

The PB1650DIO2.1 piggyback has *no* jumpers or solder straps that need to be configured.

4.6 Pin Assignment

The pin assignment of the 50-pin front-facing connector of the ES1650.1 Piggyback Carrier Board depends on whether the piggyback is mounted in position A (top) or in position B (bottom).

The pin assignment for each position of the piggyback is shown in a table.

"IN" means input channel, and "OUT" stands for output channel. The numbers indicate the channel number. "H" means handshake line.

Signal	X1 Pin	Signal	X1 Pin
PA0 OUT	33	PA0 IN	49
PA1 OUT	16	PA1 IN	32
PA2 OUT	48	PA2 IN	15
PA3 OUT	31	PA3 IN	47
PA4 OUT	14	PA4 IN	30
PA5 OUT	46	PA5 IN	13
PA6 OUT	29	PA6 IN	45
PA7 OUT	12	PA7 IN	28
H2E OUT	27	H1E IN	44
H4E OUT	43	H3E IN	11
Ext. supply voltage	50	Ext. GND	10
		Ext. GND	17
		Ext. GND	26
Ext. reset supply voltage	9	Ext. reset GND	42

Tab. 4-1 Pin Assignment of the PB1650DIO2.1 - Piggyback in Position A (Top)

Signal	X1 Pin	Signal	X1 Pin
PB0 OUT	8	PB0 IN	24
PB1 OUT	40	PB1 IN	7
PB2 OUT	23	PB2 IN	39
PB3 OUT	6	PB3 IN	22
PB4 OUT	38	PB4 IN	5
PB5 OUT	21	PB5 IN	37
PB6 OUT	4	PB6 IN	20
PB7 OUT	36	PB7 IN	3
H2E OUT	2	H1E IN	19
H4E OUT	18	H3E IN	35
Ext. supply voltage	25	Ext. GND	1
		Ext. GND	34
		Ext. GND	41
Ext. reset supply voltage	9	Ext. reset GND	42

Tab. 4-2 Pin Assignment of the PB1650DIO2.1 - Piggyback in Position B (Bottom)

4.7 Technical Data

This section contains the technical data of the PB1650DIO2.1 piggyback in tabular form.

Digital Inputs

Input channels	Eight, dc decoupled, two control lines, opto-isolated
Input voltage	5 V DC
Switching level	<1.5 V = low ≥3.0 V = high
Input current	10 mA at 5 V

Digital Outputs

Output channels	Eight, dc decoupled, two control lines, opto-isolated
Output voltage	5 V max.
Output current	10 mA max.

Channel Properties

Input frequency	500 kHz max.
Isolation voltage	2500 V RMS between input and digital ground of the VMEbus

Environmental Conditions

Ambient temperature during operation	0 to +70 °C
Storage temperature	-40 to +85 °C
Relative humidity	0 to 95% (no condensation)

Physical Dimensions

Length	100 mm
Width	48 mm
Depth	12 mm

5 PB1650ADC1.1 A/D Piggyback (8 Channels)

This section contains information about the basic features and applications of the PB1650ADC1.1 A/D piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

5.1 Features

The PB1650ADC1.1 piggyback is used for analog data acquisition in VMEbus systems in conjunction with the ES1650.1 Piggyback Carrier Board. The module is designed for medium resolutions and small to medium data rates. It has the following features:

- analog/digital conversion with 12-bit resolution and a max. sampling rate of 20 kHz
- 8 unipolar or bipolar input channels, programmed by software
- four input voltage ranges
- ID byte

5.2 Applications

The PB1650ADC1.1 piggyback can be used in VMEbus systems where analog input signals need to be acquired.

Examples of applications are:

- acquisition of analog sensor signals, such as engine temperature, oil temperature, accelerator position
- acquisition of analog output variables of the ECU, such as PMW signals
- simulation of analog sensors receiving a control or reference voltage from the ECU

5.3 Block Diagram

The following figure shows a block diagram of the PB1650ADC1.1 piggyback:

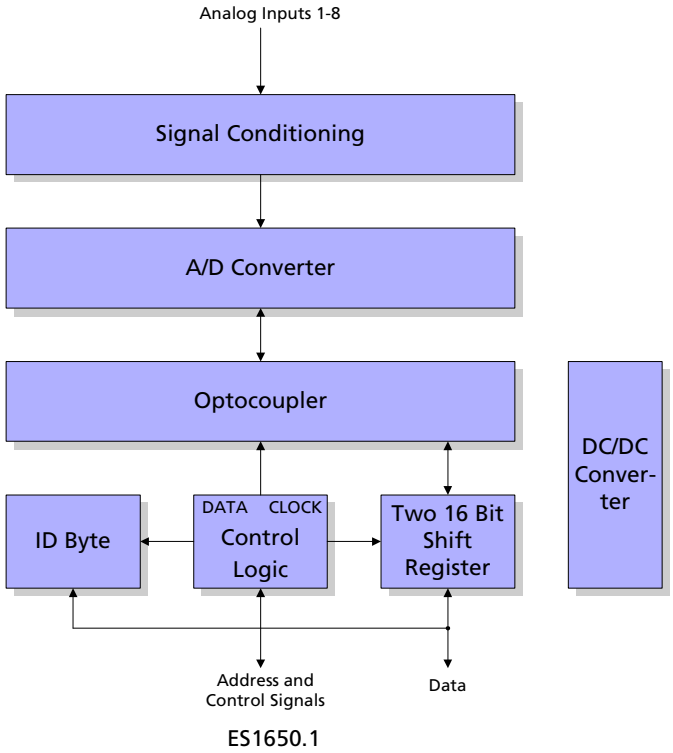


Fig. 5-1 PB1650ADC1.1 Block Diagram

At the top of the diagram, you can see the eight analog inputs, and, moving down, the signal conditioner and the analog/digital converter. The signals pass to the shift register via optocouplers (i.e. fully electrically isolated) and from there to the VMEbus interface of the basic board. The control logic is part of the piggyback. It controls the converters and shift registers, passing the data to the ES1650.1 Piggyback Carrier Board.

5.4 PB1650ADC1.1 Hardware

This section gives you a detailed overview of the features of the PB1650ADC1.1 piggyback. The following subjects are explained:

- signal conditioning
- input voltage range and gain
- analog/digital converter
- control interface
- ID byte
- size of the address range

The following figure shows the position of the components on the piggyback.

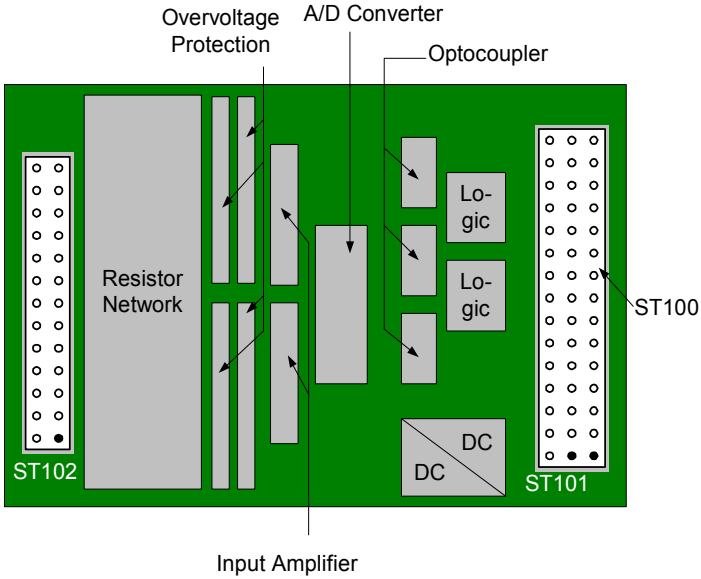


Fig. 5-2 Component Side of the PB1650ADC1.1

5.4.1 Signal Conditioning

The board has eight analog unipolar (single-ended) or bipolar inputs. Each channel has its own preamplifier.

The mode (unipolar or bipolar) can be selected for each channel using the software.

5.4.2 Input Voltage Range and Gain

The input voltage in unipolar mode is 0 V to +5 V or 0 V to +10 V. The input voltage in bipolar mode is –5 V to +5 V or –10 V to +10 V.

The input amplifier gain can be set to 0.4975 or 0.9901 for each channel using jumpers.

5.4.3 A/D Converter

The analog/digital converter features a 12-bit resolution and a max. sampling rate of 20 kHz. The conversion delay is 43 µsec.

The converter applies the successive approximation method requiring four clock cycles for each of the twelve approximation steps.

5.4.4 Control Logic

The control logic, in conjunction with the two shift registers, forms the serial interface to the A/D converter and the associated calibration component.

It also forms the status register, thus controlling the conversion time.

5.4.5 ID Byte

The control interface also generates an ID byte for the piggyback. The ID byte for the PB1650ADC1.1 piggyback is $F4. The ID byte can be used to detect the equipment of the ES1650.1 Piggyback Carrier Board using a software program.

5.4.6 Size of the Address Range

The size of the address range occupied by the PB1650ADC1.1 in your system is 256 bytes.

The B16 jumper on the ES1650.1 Piggyback Carrier Board has to be open for this address range size.

5.5 Configuration

This section contains the information for configuring the solder straps of the PB1650ADC1.1 piggyback. The following configurations can be set using solder straps:

- input voltage range
- offset voltage

The figure below shows the position of the solder straps on the solder side of the board.

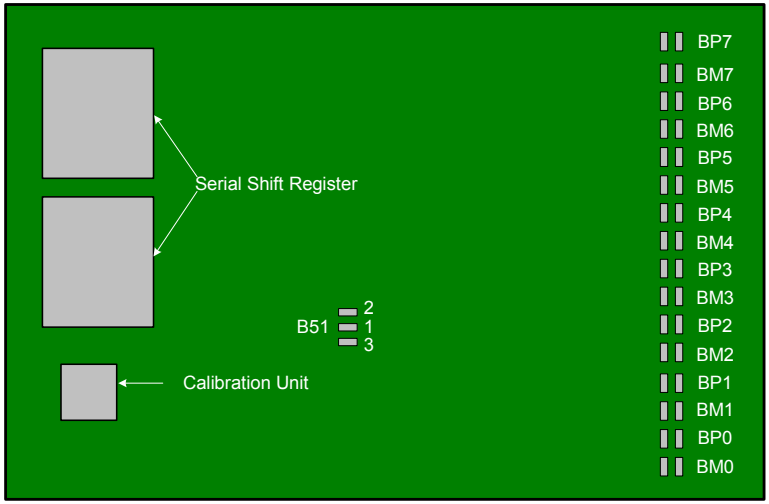


Fig. 5-3 PB1650ADC1.1 Solder Side with Solder Straps

5.5.1 Input Voltage Range

The following table describes the function of each solder strap.

Input Channel	Solder Strap	Position	Input Voltage Range
0	BP0, BM0	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
1	BP1, BM1	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
2	BP2, BM2	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
3	BP3, BM3	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
4	BP4, BM4	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V

Tab. 5-1 Input Voltage Range of the PB1650ADC1.1

Input Channel	Solder Strap	Position	Input Voltage Range
5	BP5, BM5	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
6	BP6, BM6	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V
7	BP7, BM7	Open Closed	0-10 V and +/-10 V 0-5 V and +/-5 V

Tab. 5-1 Input Voltage Range of the PB1650ADC1.1 (cont'd)

5.5.2 Offset Voltage

Use jumper B51 to select the common offset voltage for all input channels.

Solder Strap	Position	Input Voltage
B51	1-3 closed	*No* additional offset voltage at each input
B51	1-2 closed	Approx. 7.5 mV offset voltage at each input

Tab. 5-2 Offset Voltage of the PB1650ADC1.1

5.6 Pin Assignment

The pin assignment of the X1 front connector of the ES1650.1 Piggyback Carrier Board depends on whether the piggyback is mounted in position A (top) or in position B (bottom).

The pin assignment for each position of the piggyback is shown in a table.

"A" indicates the non-inverting and "B" the inverting input of the channel. If you want to measure a voltage, the signal has to be applied between connections A and B.

The number following the letter indicates the channel number.

Signal	X1 Pin	Signal	X1 Pin
A0(+)	50	B0(-)	17
A1(+)	16	B1(-)	32
A2(+)	48	B2(-)	15
A3(+)	14	B3(-)	30
A4(+)	46	B4(-)	13
A5(+)	12	B5(-)	28

Tab. 5-3 Pin Assignment of the PB1650ADC1.1 - Piggyback in Position A

Signal	X1 Pin	Signal	X1 Pin
A6(+)	44	B6(-)	11
A7(+)	10	B7(-)	26
Ext. reset supply voltage	9	Ext. reset GND	42
Ground	27	Ground	43
Ground	29	Ground	45
Ground	31	Ground	47
Ground	33	Ground	49

Tab. 5-3 Pin Assignment of the PB1650ADC1.1 - Piggyback in Position A

Signal	X1 Pin	Signal	X1 Pin
A0(+)	25	B0(-)	41
A1(+)	40	B1(-)	7
A2(+)	23	B2(-)	39
A3(+)	38	B3(-)	5
A4(+)	21	B4(-)	37
A5(+)	36	B5(-)	3
A6(+)	19	B6(-)	35
A7(+)	34	B7(-)	1
Ground	2	Ground	18
Ground	4	Ground	20
Ground	6	Ground	22
Ground	8	Ground	24

Tab. 5-4 Pin Assignment of the PB1650ADC1.1 - Piggyback in Position B

5.7 Technical Data

This section contains the technical data of the PB1650ADC1.1 analog/digital converter piggyback in tabular form.

Analog/Digital Converter

Resolution	12-bit
Conversion delay	43 µs
Sampling rate	20 kHz
Linearity	+/-0.75 LSB

Analog Input

Analog channels	8
Input resistance	In the 5 V range: 20 KΩ In the 10 V range: 40 KΩ
Overvoltage protection	+/- 35 V continuous
Input voltage	Unipolar: 0 to 5 V, 0 to 10 V Bipolar: +/-5 V, +/-10 V

Environmental Conditions

Ambient temperature during operation	0 to +70 °C

Physical Dimensions

Length	100 mm
Width	48 mm
Depth	12 mm

6 PB1650REL1.1 Relay Piggyback (8 Channels)

This section contains information about the basic features and applications of the PB1650REL1.1 relay piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

note

The components, connectors, and printed lines of the piggyback may carry dangerous high voltages.
These voltages may even exist when the piggyback is not installed in the VME system or when the VME system is powered off.
Make sure that the piggyback is protected against contact during its operation.
Disconnect all connections to the ES1650.1 Piggyback Carrier Board before removing the plug-in board from the VME system.

6.1 Features

This piggyback provides eight electrically isolated switches in the voltage range up to 175 V.

The piggyback has the following features:

- voltages up to 175 V, currents up to 250 mA
- its own ID byte

6.2 Applications

The PB1650REL1.1 piggyback can be used in VMEbus systems as a switch in conjunction with the ES1650.1 Piggyback Carrier Board.

Typical applications are the simulation of manual switches or the switching of loads that cannot be switched using semiconductor switches. The PB1650REL1.1 piggyback can also be used as an analog multiplexer.

6.3 Block Diagram

The block diagram below illustrates the working principle of the module.

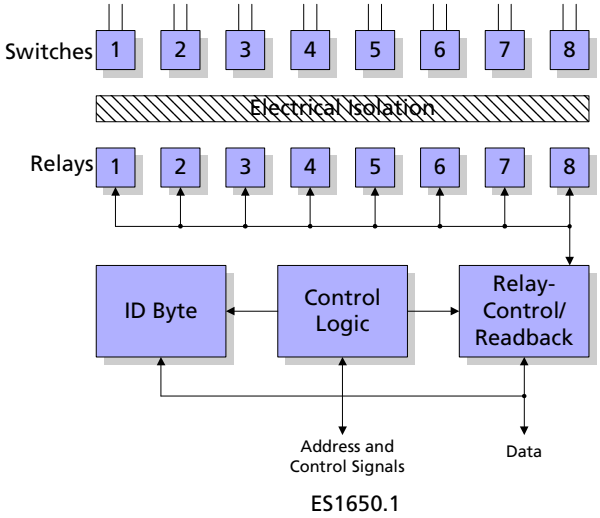


Fig. 6-1 PB1650REL1.1 Block Diagram

At the top, adjacent to the user side, you can see eight relay change-over switches, electrically isolated from each other and from the VMEbus system. Their switching states are detected by the logic in the bottom center. The function of the relays is controlled by a separate control interface on the module. In addition, the PB1650REL1.1 has its own ID, as can be seen on the extreme left of the block diagram. This end of the board is also where the board is connected to the VMEbus via the interface to the ES1650.1 Piggyback Carrier Board.

6.4 PB1650REL1.1 Hardware

This section gives you a detailed overview of the features of the PB1650REL1.1 piggyback. You will find information on the following subjects:

- relays
- output voltage range
- ID byte and address
- size of the address range

The following figure shows the position of the components on the component side of the piggyback.

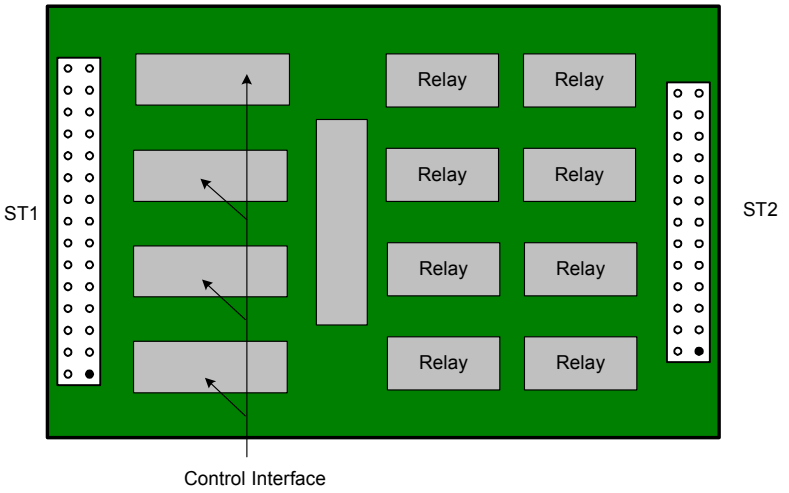


Fig. 6-2 Component Side of the PB1650REL1.1

6.4.1 Relays

The relay piggyback has eight relays. The contacts are electrically isolated from each other and from the VMEbus system. Each relay is equipped with a change-over switch.

6.4.2 Output Voltage Range

The relays are capable of switching up to 175 V DC and 250 mA. The maximum switching power is 3 W per contact.

6.4.3 ID Byte

The ID byte of the PB1650REL1.1 piggyback is "$FC". The ID byte can be used to detect the equipment of the ES1650.1 Piggyback Carrier Board using a software program.

6.4.4 Size of the Address Range

The size of the address range occupied by the PB1650REL1.1 in your system is 256 bytes.

The B16 jumper on the ES1650.1 Piggyback Carrier Board has to be open for this address range size.

6.5 Configuration

The PB1650REL1.1 piggyback has *no* jumpers or solder straps that need to be configured.

6.6 Pin Assignment

The pin assignment of the ES1650.1 Piggyback Carrier Board depends on whether the piggyback is mounted in position A (top) or in position B (bottom).

The pin assignment for each position of the piggyback is shown in a table.

Key to abbreviations:

- Pole: center contact
- NC: normally closed
- NO: normally open

The number indicates the channel number.

Signal	X1 Pin	Signal	X1 Pin
Relay 0 NC	49	Relay 0 NO	50
Relay 1 NC	48	Relay 1 NO	16
Relay 2 NC	47	Relay 2 NO	15
Relay 3 NC	46	Relay 3 NO	14
Relay 4 NC	45	Relay 4 NO	13
Relay 5 NC	44	Relay 5 NO	12
Relay 6 NC	43	Relay 6 NO	11

Tab. 6-1 Pin Assignment of the PB1650REL1.1 - Piggyback in Position A (Top)

Signal	X1 Pin	Signal	X1 Pin
Relay 7 NC	17	Relay 7 NO	10
Relay 0 Pole	33	Relay 4 Pole	29
Relay 1 Pole	32	Relay 5 Pole	28
Relay 2 Pole	31	Relay 6 Pole	27
Relay 3 Pole	30	Relay 7 Pole	26
Ext. reset supply voltage	9	Ext. reset GND	42

Tab. 6-1 Pin Assignment of the PB1650REL1.1 - Piggyback in Position A (Top) (cont'd)

Signal	X1 Pin	Signal	X1 Pin
Relay 0 NC	24	Relay 0 NO	25
Relay 1 NC	23	Relay 1 NO	40
Relay 2 NC	22	Relay 2 NO	39
Relay 3 NC	21	Relay 3 NO	38
Relay 4 NC	20	Relay 4 NO	37
Relay 5 NC	19	Relay 5 NO	36
Relay 6 NC	18	Relay 6 NO	35
Relay 7 NC	41	Relay 7 NO	34
Relay 0 Pole	8	Relay 4 Pole	4
Relay 1 Pole	7	Relay 5 Pole	3
Relay 2 Pole	6	Relay 6 Pole	2
Relay 3 Pole	5	Relay 7 Pole	1

Tab. 6-2 Pin Assignment of the PB1650REL1.1 - Piggyback in Position B (Bottom)

6.7 Technical Data

This section contains the technical data of the PB1650REL1.1 piggyback in tabular form.

Outputs

Number of output channels	8 (electrically isolated)
Switching voltage	Max. 175 V DC
Switching current	Max. 250 mA
Switching power	Max. 3 W per relay
Switching time	< 3 msec

Power Supply

Supply voltage	+5 V (±5 %)
Supply current	100 mA + 22.5 mA per activated channel

Environmental Conditions

Ambient temperature during operation	0 to +70 °C
Storage temperature	-55 to +85 °C
Relative humidity	0 to 95 % no condensation

Physical Dimensions

Length	100 mm
Width	48 mm
Depth	12 mm

7 PB1650PRT1.1 Prototyping Piggyback

This section contains information about the basic features and applications of the PB1650PRT1.1 Prototyping Piggyback. A block diagram shows the schematic layout of the module.

note

Some components of the piggyback may be damaged or destroyed by electrostatic discharges. Please keep the piggyback in its storage package until it is installed.
The piggyback should only be taken from its storage package, configured and installed at a work place that is protected against static discharge.

7.1 Features

The PB1650PRT1.1 Prototyping Piggyback is used for constructing circuits in a wrap area. You can mount the ES4060.1 processor module on the prototyping piggyback to execute universal control tasks.

The piggyback has the following features:

- wrap area that can be equipped individually to suit your applications

The following functions are also available to you in conjunction with the optional ES4060.1 processor module:

- serial FLASH memory
- Dual-Ported RAM for data transfer from and to the VMEbus

note

The PB1650PRT1.1 Prototyping Piggyback takes up both slots for piggybacks on the ES1650.1 Piggyback Carrier Board.

7.2 Applications

The PB1650PRT1.1 Prototyping Piggyback is used in conjunction with the ES1650.1 Piggyback Carrier Board in VMEbus systems to develop various circuits.

Examples of application areas are:

- with ES4060.1 processor module: development of complex microprocessor-based control and data acquisition circuits which use analog, digital or PWM inputs and outputs, a VMEbus or a CANbus interface
- without ES4060.1 processor module: development of circuits for signal conditioning

The PB1650PRT1.1 Prototyping Piggyback is normally used with the ES4060.1 Processor Module. The processor module makes a range of I/O, PWM and A/D channels, and various interfaces such as SPI, CAN, JTAG etc. available. These can be addressed using the VMEbus or CAN interface. For more information on programming the interfaces and peripheral units as well as on data exchange using the VMEbus and the CAN interface, please refer to the firmware manual on the ES4060.1 Processor Module.

The block diagram below illustrates the working principle of the PB1650PRT1.1 Piggyback.

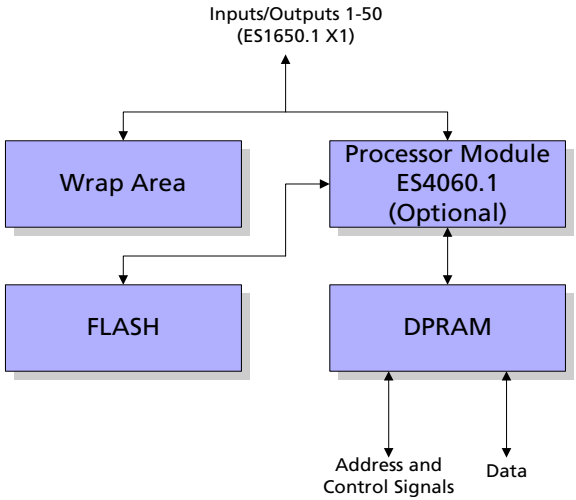


Fig. 7-1 PB1650PRT1.1 Block Diagram

At the top of the diagram you can see the X1 connector and the inputs and outputs of the ES1650.1 Piggyback Carrier Board. If you develop circuits with the ES4060.1 Processor Module, the signals are transferred to the VMEbus interface on the carrier board via the processor module and the Dual-Ported RAM (DPRAM).

Configuration data for the processor module and user-specific data are stored in the Flash memory.

The wrap area is available for constructing individual circuits.

Both the wrap area and the ES4060.1 Processor Module have common connections to the carrier board's front-facing connector, X1.

The figure below shows a side view of the mechanical structure of the three circuits on the board.

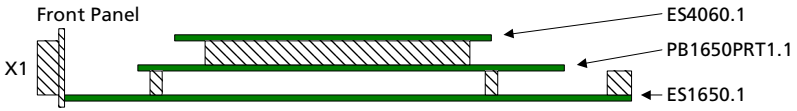


Fig. 7-2 Mechanical Structure of the ES1650.1, PB1650PRT1.1 and ES4060.1

7.3 PB1650PRT1.1 Hardware

This section gives you a detailed overview of the features of the PB1650PRT1.1 Prototyping Piggyback. You will find information on the following subjects:

- supply voltages
- interfaces
- Dual-Ported RAM access
- size of the address range

The following figure shows the position of the components on the component side of the prototyping piggyback.

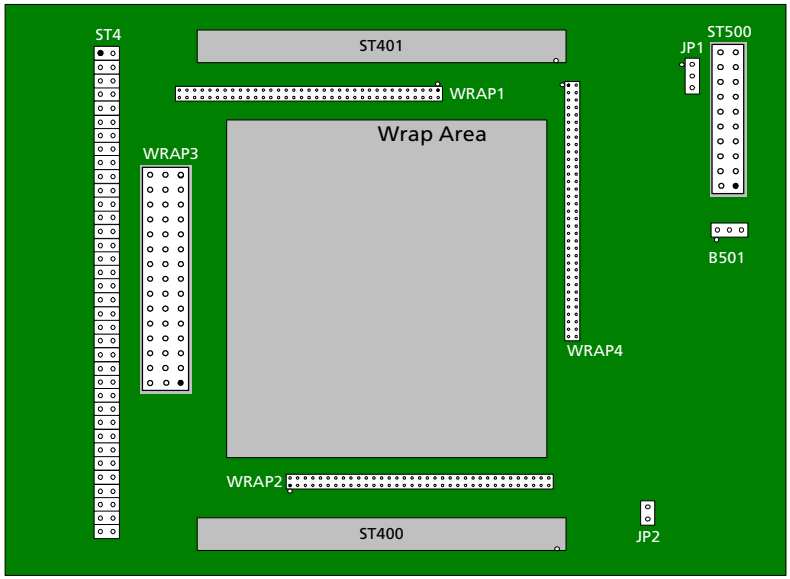


Fig. 7-3 Component Side of the PB1650PRT1.1

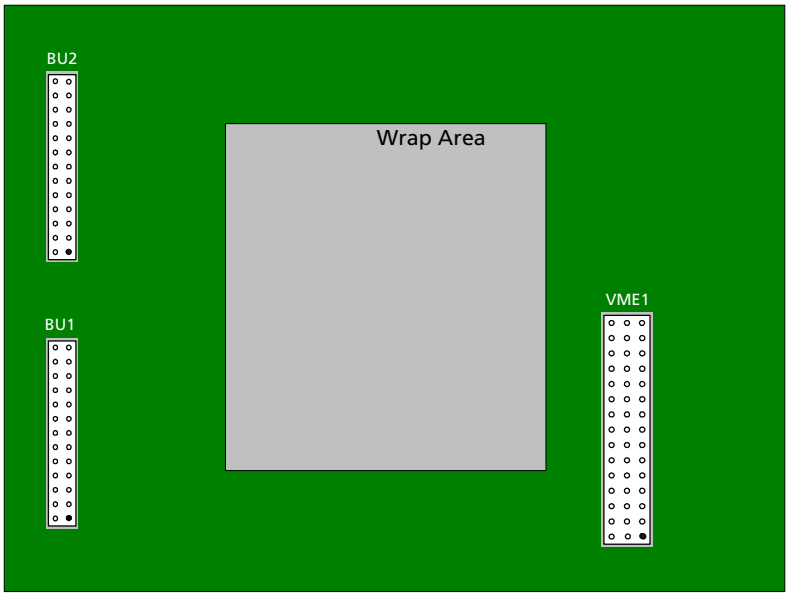


Fig. 7-4 Solder Side of the PB1650PRT1.1

7.3.1 Supply Voltages

The prototyping module makes supply voltages of +3.3 V and +5 V available. The voltages are available at pins on the wrap area and at the X1 connector on the front panel of the ES1650.1 Piggyback Carrier Board.

note

*The supply voltages are **not** protected against short-circuits and overvoltage. Short-circuits on the wrap area or on the front-facing connector can damage the PB1650PRT1.1, the ES1650.1 Piggyback Carrier Board and the ES4060.1 Processor Module.*
To avoid damage to the components, make sure that the circuits on the prototyping module are wired correctly before switching on the supply voltage.

7.3.2 VMEbus Interface

There is direct access to the 4-KByte Dual-Ported RAM area via the VMEbus interface. The address range within the VMEbus address range is determined by the configuration of the base address of the ES1650.1 Piggyback Carrier Board.

7.3.3 Dual-Ported RAM Access

The data is transferred between the VMEbus and the PB1650PRT1.1 module using a 2048 K x 16-bit Dual-Ported RAM memory.

Only 16-bit VMEbus accesses to the DPRAM are possible.

Only 32-bit accesses are admissible from the MPC555 to the 16-bit DPRAM due to the different data bus access modes of MPC555 and VMEbus with 8-bit, 16-bit and 32-bit accesses and an inconsistent connection of the 16-bit Dual-Ported RAM component. The most significant 16 bits have an undefined value in read operations and have to be masked out (e.g. with a logical 'AND' with 0x0000FFFF). The relevant 16-bit words are on the VMEbus, which can only make 16-bit accesses to the DPRAM, each at an interval of 32 bits, i.e. only to even DPRAM addresses.

DPRAM Address	MPC555 32-Bit Access	VME 16-Bit Access
0	Byte 0	Byte 0
1	Byte 1	Byte 1
2	Undef.	Undef.
3	Undef.	Undef.
4	Byte 2	Byte 2
5	Byte 3	Byte 3
6	Undef.	Undef.
7	Undef.	Undef.
...	...	...

A standard storage interface from the VMEbus and MPC555 can be realized by using C macros for 8-bit, 16-bit and 32-bit accesses.

The two examples below are two C macros for the 16-bit read and write access of the MPC555 to the DPRAM. Only a slight adaptation is necessary for accessing even addresses. When accessing odd addresses, there has to be a division into bytes:

```
#define DPR_W16B(Adr,Dat) {\
    if ((Adr) & 0x1) {\
        *(volatile uint32*)(DPRam_Adr+\
        (((Adr)-1)<<1)) = (((Dat)&0xFF00) >>8) |\

        (*(volatile uint32*)(DPRam_Adr+\
        (((Adr)-1)<<1)) & 0xFF00);\

        *(volatile uint32*)(DPRam_Adr+\
        (((Adr)+1)<<1)) = (((Dat)&0xFF) <<8) |\

        (*(volatile uint32*)(SPRam_Adr+\
        (((Adr)+1)<<1)) & 0xFF);\
    }\
    else
        *(volatile uint32*)(DPRam_Adr+\
        ((Adr)<<1)) = Dat;\
}

#define DPR_R16B(Adr) ((Adr) & 0x1) ?\
    ((*(volatile uint32*)(DPRam_Adr+(((Adr)-1)<<1)) &\
    0x00FF) << 8)+\
    ((*(volatile uint32*)(DPRam_Adr+(((Adr)+1)<<1)) &\
    0xFF00) >> 8); :\
    *(volatile uint32*)(DPRam_Adr+((Adr)<<1)) & 0xFFFF
```

7.3.4 Size of the Address Range

The size of the address range occupied by the PB1650PRT1.1 in your system is 8 KBytes.

The B16 jumper on the ES1650.1 Piggyback Carrier Board has to be closed for this address range size.

7.4 Configuration

This section contains information on configuring the jumpers of the PB1650PRT1.1 Piggyback.

The jumpers are used to configure the hardware of the PB1650PRT1.1 module.

7.4.1 B501 Jumper

The write protection of the serial Flash memory is configured with jumper B501.

B501 Jumper	Means
Pin 1-2 closed	Programming of the serial Flash memory with the ES4060.1 Processor Module or via the programming interface
Pin 3-2 closed	Programming of the serial Flash memory only via the programming interface

Tab. 7-1 B501 Jumper

The default setting for Pins 1-2 is closed.

7.4.2 JP1 Jumper

Jumper JP1 determines the speed of the DPRAM access from the VMEbus.

JP1 Jumper	Means
Pin 1-2 closed	65 ns acknowledge
Pin 3-2 closed	35 ns acknowledge

Tab. 7-2 JP1 Jumper

The default setting for Pins 3-2 is closed.

7.4.3 JP2 Jumper

The JP2 jumper configures the JTAG chain. If JTAG components are used on the wrap area, the JTAG chain can be opened to make the integration of these components in the configuration of the default JTAG chain possible. The JTAG signals are made available via the WRAP connector.

JP2 Jumper	Means
Closed	Standard JTAG chain without additional JTAG components
Open	JTAG chain opened, the chain has to be connected to the relevant ports using additional JTAG components.

Tab. 7-3 JP2 Jumper

The jumper is closed in the default setting.

7.4.4 ST4 Jumper Strip

The ST4 jumper strip configures the connection of the signals of the ES4060.1 Processor Module to the X1 front-facing connector of the ES1650.1 Piggyback Carrier Board. A connector that is plugged in means that the relevant signal of the ES4060.1 Processor Module is transferred to the selected pin of the front-facing connector.

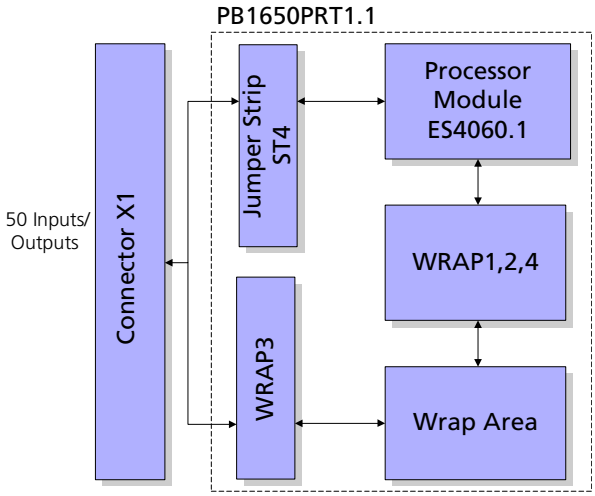


Fig. 7-5 Block Diagram - X1 Signals

All jumpers are closed in the default setting.

For more detailed information on the assignment of the connector pins, please refer to the section "Pin Assignment" on page 71.

note

The relevant jumper has to be removed to transfer user-defined signals from circuits on the wrap area to the X1 front-facing connector and to separate the connection of the ES4060.1 Processor Module and the X1 front-facing connector.

7.5 Pin Assignment

The following section contains information on the features of the individual connectors and the assignment of the pins.

Connector	Function
BU1, BU2, VME1	Contacts ES1650.1 carrier board
ST400, ST401	Contacts ES4060.1 Processor Module
WRAP1-WRAP4	Contacts wrap area
ST500	JTAG interface (programming interface)
ST4	Jumper strip for the connection between ES4060.1, the front-facing connector X1 and the WRAP3 wrap area

7.5.1 ES1650.1 X1 Front-Facing Connector

The table in this section contains the pin assignment of the 50-pin front-facing connector X1 of the ES1650.1 Piggyback Carrier Board as well as information on the signals of the ES4060.1 Processor Module, the assignment of the associated pin of the ST4 jumper strip, the associated pin of the WRAP3 connector and the assignment of the relevant WRAP connector and its pin.

note

For information on the functions of the ES4060.1 Processor Module pins, please refer to the MPC555 Microprocessor manual. The MPC555 user manual can be accessed online at: http://mot-sps.com/mcu/documentation/mpc5xx/mpc5db.html

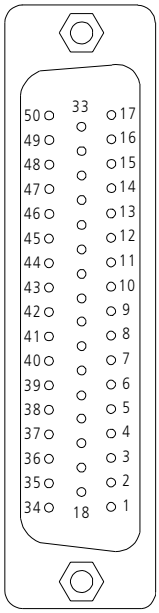


Fig. 7-6 X1 Front-Facing Connector

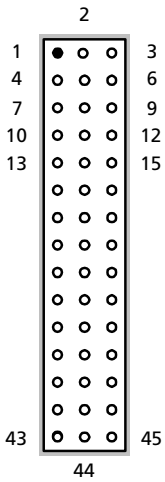


Fig. 7-7 WRAP3 Wrap Area

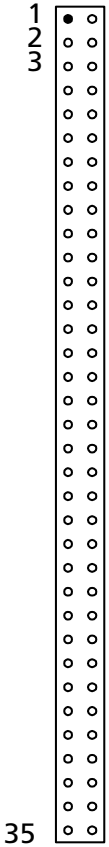


Fig. 7-8 ST4 Jumper Strip

X1 Pin	Signal of the ES4060.1 when Jumper Closed	Associated Pin of the ST4 Jumper Strip	Associated Pin of the WRAP3 Connector	WRAP Connector and Pin
1	GND (fixed)	n. c.	n. c.	n. c.
2	PDA0	35	1	Wrap2 Pin 66
3	PDA1	34	2	Wrap2 Pin 65
4	PDA2	33	3	Wrap2 Pin 64
5	PDA3	32	4	Wrap2 Pin 63

Tab. 7-4 Pin Assignment of the PB1650PRT1.1

X1 Pin	Signal of the ES4060.1 when Jumper Closed	Associated Pin of the ST4 Jumper Strip	Associated Pin of the WRAP3 Connector	WRAP Connector and Pin
6	PDA4	31	5	Wrap2 Pin 62
7	PDA5	30	6	Wrap2 Pin 61
8	PDA6	29	7	Wrap2 Pin 60
9	Reset/GND	n. c.	n. c.	n. c.
10	PDA7	28	8	Wrap2 Pin 59
11	PDA8	27	9	Wrap2 Pin 58
12	PTPUB0	26	10	Wrap4 Pin 23
13	PTPUA0	25	11	Wrap4 Pin 7
14	PETRIG1	24	12	Wrap2 Pin 67
15	PETRIG2	23	13	Wrap2 Pin 68
16	PANB0	22	14	Wrap1 Pin 15
17	PANB1	21	15	Wrap1 Pin 16
18	VDD15 analog reference	20	16	Wrap1 Pin 14
19	PPWM0	19	17	Wrap1 Pin 47
20	PPWM1	18	18	Wrap1 Pin 48
21	/BPIRQ7	17	19	Wrap2 Pin 57
22	PANA0	16	20	Wrap1 Pin 31
23	PANA1	15	21	Wrap1 Pin 32
24	PANA2	14	22	Wrap1 Pin 33
25	PANA3	13	23	Wrap1 Pin 34
26	PANA4	12	24	Wrap1 Pin 35
27	PANA5	11	25	Wrap1 Pin 36
28	PANA6	10	26	Wrap1 Pin 37
29	PANA7	9	27	Wrap1 Pin 38
30	PANA8	8	28	Wrap1 Pin 39
31	PANA9	7	29	Wrap1 Pin 40
32	PANA10	6	30	Wrap1 Pin 41
33	PANA11	5	31	Wrap1 Pin 42
34	PANA12	4	32	Wrap1 Pin 43

Tab. 7-4 Pin Assignment of the PB1650PRT1.1 (cont'd)

X1 Pin	Signal of the ES4060.1 when Jumper Closed	Associated Pin of the ST4 Jumper Strip	Associated Pin of the WRAP3 Connector	WRAP Connector and Pin
35	PANA13	3	33	Wrap1 Pin 44
36	PANA14	2	34	Wrap1 Pin 45
37	PANA15	1	35	Wrap1 Pin 46
38	User-defined	n. c.	36	n. c.
39	User-defined	n. c.	37	n. c.
40	User-defined	n. c.	38	n. c.
41	User-defined	n. c.	39	n. c.
42	Reset/VCC	n. c.	n. c.	n. c.
43	User-defined	n. c.	40	n. c.
44	RTS (RS232)	n. c.	41	n. c.
45	CTS (RS232)	n. c.	42	n. c.
46	RXD (RS232)	n. c.	43	n. c.
47	TXD (RS232)	n. c.	44	n. c.
48	CAN-L	n. c.	n. c.	n. c.
49	CAN-H	n. c.	n. c.	n. c.
50	VCC +5 V	n. c.	n. c.	n. c.
n. c.	GND	n. c.	45	n. c.

Tab. 7-4 Pin Assignment of the PB1650PRT1.1 (cont'd)

7.5.2 WRAP1 Connector

Processor module signals are made available on the wrap area via the WRAP1 connector.

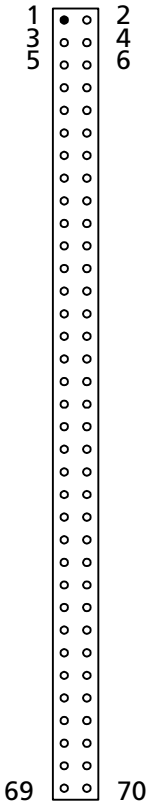


Fig. 7-9 Pin Assignment of WRAP1, WRAP2 and WRAP4

Pin	Signal	X1	Pin	Signal	X1
1	VCC +5 V	50	2	VCC +5 V	50
3	VCC +3.3 V	n. c.	4	VCC +3.3 V	n. c.
5	ACNBRX	n. c.	6	ACNBTX	n. c.
7	ARXD2	n. c.	8	ATXD2	n. c.
9	/PSRESET	n. c.	10	/PHRESET	n. c.

Tab. 7-5 Pin Assignment of the PB1650PRT1.1 - WRAP1 Connector

Pin	Signal	X1	Pin	Signal	X1
11	/PPORESET	n. c.	12	PCLKOUT	n. c.
13	PECK	n. c.	14	VDD15	18
15	PANB0	16	16	PANB1	17
17	PANB2	n. c.	18	PANB3	n. c.
19	PANB4	n. c.	20	PANB5	n. c.
21	PANB6	n. c.	22	PANB7	n. c.
23	PANB8	n. c.	24	PANB9	n. c.
25	PANB10	n. c.	26	PANB11	n. c.
27	PANB12	n. c.	28	PANB13	n. c.
29	PANB14	n. c.	30	PANB15	n. c.
31	PANA0	22	32	PANA1	23
33	PANA2	24	34	PANA3	25
35	PANA4	26	36	PANA5	27
37	PANA6	28	38	PANA7	29
39	PANA8	30	40	PANA9	31
41	PANA10	32	42	PANA11	33
43	PANA12	34	44	PANA13	35
45	PANA14	36	46	PANA15	37
47	PPWM0	19	48	PPWM1	20
49	PPWM2	n. c.	50	PPWM3	n. c.
51	PPWM4	n. c.	52	PPWM5	n. c.
53	PPWM6	n. c.	54	PPWM7	n. c.
55	MPIO2	n. c.	56	MPIO3	n. c.
57	MPIO4	n. c.	58	MPIO5/TDO	n. c.
59	MPIO6/TDI	n. c.	60	MPIO7/TCK	n. c.
61	MPIO8/TMS	n. c.	62	MPIO9/CSBP	n. c.
63	MPIO10	n. c.	64	MPIO11	n. c.
65	MPIO12	n. c.	66	MPIO13	n. c.
67	MPIO14	n. c.	68	MPIO15	n. c.
69	GND	1	70	GND	1

Tab. 7-5 Pin Assignment of the PB1650PRT1.1 - WRAP1 Connector

7.5.3 WRAP2 Connector

Processor module bus signals are made available on the wrap area via the WRAP2 connector. (For details of the pin assignment see the section "Pin Assignment of WRAP1, WRAP2 and WRAP4" on page 76)

Pin	Signal	X1	Pin	Signal	X1
1	PA23	n. c.	2	PA22	n. c.
3	PA21	n. c.	4	PA20	n. c.
5	PA19	n. c.	6	PA18	n. c.
7	PA17	n. c.	8	PA16	n. c.
9	PA15	n. c.	10	PA14	n. c.
11	PA13	n. c.	12	PA12	n. c.
13	PA11	n. c.	14	PA10	n. c.
15	PA9	n. c.	16	PA8	n. c.
17	PA7	n. c.	18	PA6	n. c.
19	PA5	n. c.	20	PA4	n. c.
21	PA3	n. c.	22	PA2	n. c.
23	PA1	n. c.	24	PA0	n. c.
25	PD15	n. c.	26	PD14	n. c.
27	PD13	n. c.	28	PD12	n. c.
29	PD11	n. c.	30	PD10	n. c.
31	PD9	n. c.	32	PD8	n. c.
33	PD7	n. c.	34	PD6	n. c.
35	PD5	n. c.	36	PD4	n. c.
37	PD3	n. c.	38	PD2	n. c.
39	PD1	n. c.	40	PD0	n. c.
41	/PWE	n. c.	42	/PCS3	n. c.
43	/POE	n. c.	44	/PBE0	n. c.
45	/PBE1	n. c.	46	TMS	n. c.
47	TCK	n. c.	48	TDI	n. c.
49	TDO	n. c.	50	/PCS2	n. c.
51	QMISO	n. c.	52	QSCK	n. c.
53	QMOSI	n. c.	54	/QCS3	n. c.

Tab. 7-6 Pin Assignment of the PB1650PRT1.1 - WRAP2 Connector

Pin	Signal	X1	Pin	Signal	X1
55	/QCS2	n. c.	56	/QCS1	n. c.
57	/BPIRQ7	21	58	PDA8	11
59	PDA7	10	60	PDA6	8
61	PDA5	7	62	PDA4	6
63	PDA3	5	64	PDA2	4
65	PDA1	3	66	PDA0	2
67	PETRIG1	14	68	PETRIG2	15
69	Reserved	n. c.	70	Reserved	n. c.

Tab. 7-6 Pin Assignment of the PB1650PRT1.1 - WRAP2 Connector

7.5.4 WRAP4 Connector

Signals of the processor module are made available on the wrap area via the WRAP4 connector. (For details of the pin assignment see the section "Pin Assignment of WRAP1, WRAP2 and WRAP4" on page 76)

Pin	Signal	X1	Pin	Signal	X1
1	VCC +5 V	50	2	VCC +5 V	50
3	VCC +3.3 V	n. c.	4	VCC +3.3 V	n. c.
5	/AIRQOUT	n. c.	6	Reserved	n. c.
7	PTPUA0	13	8	PTPUA1	n. c.
9	PTPUA2	n. c.	10	PTPUA3	n. c.
11	PTPUA4	n. c.	12	PTPUA5	n. c.
13	PTPUA6	n. c.	14	PTPUA7	n. c.
15	PTPUA8	n. c.	16	PTPUA9	n. c.
17	PTPUA10	n. c.	18	PTPUA11	n. c.
19	PTPUA12	n. c.	20	PTPUA13	n. c.
21	PTPUA14	n. c.	22	PTPUA15	n. c.
23	PTPUB0	12	24	PTPUB1	n. c.
25	PTPUB2	n. c.	26	PTPUB3	n. c.
27	PTPUB4	n. c.	28	PTPUB5	n. c.
29	PTPUB6	n. c.	30	PTPUB7	n. c.
31	PTPUB8	n. c.	32	PTPUB9	n. c.

Tab. 7-7 Pin Assignment of the PB1650PRT1.1 - WRAP4 Connector

Pin	Signal	X1	Pin	Signal	X1
33	PTPUB10	n. c.	34	PTPUB11	n. c.
35	PTPUB12	n. c.	36	PTPUB13	n. c.
37	PTPUB14	n. c.	38	PTPUB15	n. c.

Tab. 7-7 Pin Assignment of the PB1650PRT1.1 - WRAP4 Connector

7.5.5 ST500 Connector

Signals for programming serial Flash memories and PLD are made available via the ST500 connector.

Pin	Signal	Pin	Signal
1	TCK	2	GND
3	TDO	4	Supply voltage +5 V
5	TMS	6	DONE
7	CCLK	8	INIT
9	TDI	10	GND
11	/DFCS	12	DFSCK
13	GND	14	DIN_DFSO
15	GND	16	DFSI
17	/DFWP	18	EXT_EN_PROG
19	Supply voltage +3.3 V	20	/PROG

Tab. 7-8 Pin Assignment of the PB1650PRT1.1 - ST500 Connector

7.6 Technical Data

This section contains the technical data of the PB1650PRT1.1 piggyback in tabular form.

Electrical Data

Supply voltages for prototype circuits and ES4060	+3.3 V; +5 V
Supply current for prototype circuits and ES4060	Max. 250 mA at +3.3 V Max. 500 mA at +5 V
Supply current from ES1650	Max. 1 A at +5 V

Physical Dimensions

Length	134.6 mm
Width	100.0 mm

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List of Figures

List of Tables

Index

E

F

G

I

O

P

R

S

V

W