



Product:	ETK11.0	Rev :	01	Page 1 of 8
Title :	Change Information			

Product :	ETK11.0			
Title :	Change Information			
File :	ETK11.0_Change_Information_V01.doc			
TTN :	F-00K-102-632			
Comments :	Currently shipped: <b>1124B010</b> EPLD version: V11 FPGA version: V24 Hardware-state: B010			
Created:	Name Higgins	Department PHW-EPM31	Signature Higgins	Date 14.11.2006
Released:	Name Collins	Department PHW-EPM32	Signature Collins	Date 16.11.2006
<b>C h a n g e s</b>				
Revision	Description	Date	Name	Signature
01	1124B010 - initial version	14.11.2006	Higgins	Higgins

Product:	ETK11.0	Rev :	01	Page 2 of 8
Title :	Change Information			

## Table of Contents

1	General remarks to this document.....	3
2	Tool-Chain Information.....	4
2.1	Version-Syntax of the ETK11.0.....	4
2.2	Version information of the Tool-Chain components.....	5
3	PLD-Code Changes.....	6
3.1	General remarks to this chapter.....	6
3.2	EPLD-Code version 1.1 was the first delivered version.....	6
3.2.1	No change.....	6
3.2.2	Delivery condition.....	6
3.3	FPGA-Code version 2.4 was the first delivered version.....	6
3.3.1	No change.....	6
3.3.2	Delivery condition.....	6
4	Hardware Changes.....	7
4.1	General remarks to this chapter.....	7
4.2	No changes from version B010.....	7
4.2.1	Delivery condition.....	7
5	Abbreviations.....	8

Product:	ETK11.0	Rev :	01	Page 3 of 8
Title :	Change Information			

## 1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.

Two different items are described.

- Explanation of the version-system of the ETK11.0
- The required versions of software (INCA / ASCET / INTECRIO), HSP (calibration hardware firmware of e.g. ES59x, ES690, ES1232, ...) and ETK - hardware. Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

Product:	ETK11.0	Rev :	01	Page 4 of 8
Title :	Change Information			

## 2 Tool-Chain Information

### 2.1 Version-Syntax of the ETK11.0

The ETK11.0 version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: **aabbccddd/ee**

PLD-Code Information:

**aa:** EPLD-Code version (10, 11, 12...) see chapter 3

**bb:** FPGA-Code version (10, 11, 12...) see chapter 3

Hardware-Information:

**c:** PCB version (A, B, C, ...)

**ddd:** Hardware state of the PCB (010, 011, 012, ...) see chapter 4

**ee:** Assembly variant of the PCB (00, 01, 02, ...)

The first delivered hardware state of the ETK11.0 was **1124B010/00**.

Product:	ETK11.0	Rev :	01	Page 5 of 8
Title :	Change Information			

## 2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.

If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
HSP	V5.1	
ES690	V10.1.0	Supported
ES59x	V10.1.0	Supported
ES910.2	HSP V5.1.1	Supported
ES1000.2/3 – system	V10.1.0	Supported with ES1232
MAC2, ES1000.1, ES1200/01, and ES1231		Not supported
<b>Software</b>		
INCA	V5.4.1	
ASCET-RP	V5.5	
INTECRIO	V2.1	

List of officially supported Freescale microcontrollers:

- MPC5554
- MPC5553
- MPC5565
- MPC5566

The registered user will automatically receive the newest INCA-version (CD-ROM)

Updates or refreshes can be downloaded from the ETAS homepage:

<http://de.etasgroup.com>

<http://en.etasgroup.com>

Product:	ETK11.0	Rev :	01	Page 6 of 8
Title :	Change Information			

### 3 PLD-Code Changes

#### 3.1 General remarks to this chapter

The programmable logic code within the ETK11.0 is stored onto programmable logic devices (FPGA and EPLD). For the version syntax please refer to chapter 2.1.

#### 3.2 EPLD-Code version 1.1 was the first delivered version

##### 3.2.1 No change

**Version 1.1:** file dated 06.09.2006

##### 3.2.2 Delivery condition

The EPLD version **1.1** will be programmed into all new shipments.

#### 3.3 FPGA-Code version 2.4 was the first delivered version

##### 3.3.1 No change

**Version 2.4:** file dated 15.11.2006

##### 3.3.2 Delivery condition

The FPGA version **2.4** will be programmed into all new shipments.

Product:	ETK11.0	Rev :	01	Page 7 of 8
Title :	Change Information			

## 4 Hardware Changes

### 4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes is listed underneath. The hardware-state starts with version B010. For the version syntax please refer to chapter 2.1.

### 4.2 No changes from version B010

#### 4.2.1 Delivery condition

The hardware-state **B010** will be delivered with all new shipments.  
ETKs with 'older' hardware-states can be modified to the current valid state.

Product:	ETK11.0	Rev :	01	Page 8 of 8
Title :	Change Information			

## 5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	<b>H</b> ardware <b>S</b> ervice <b>P</b> ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	<b>M</b> easurement & <b>C</b> alibration
RP	<b>R</b> apid <b>P</b> rototyping
PLD	<b>P</b> rogrammable <b>L</b> ogic <b>D</b> evice
FPGA	<b>F</b> ree <b>P</b> rogrammable <b>G</b> ate <b>A</b> rray; interface component to the application hardware
PCB	<b>P</b> rinted <b>C</b> ircuit <b>B</b> oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select