Product :	ETK7.1
Title :	Change Information
File :	ETK71 Change_Information_V14.doc
TTN :	F-00K-001-475 – ETK7.1
Comments :	Currently shipped: **1220B011** EPLD-Code version: V 1.2 FPGA-Code version: V 2.0 Hardware-state: B011

	Name	Department	Signature	Date
Created:	Mai	PGA/PRM-H	Mai	10.11.2011
Checked:	Hofmeier	NE/EPM1	Hofmeier	11.11.2011

C h a n g e s

Revision	Description	Date	Name	Signature
1.0	1011B010/00 - Initial Version	..	Colling	Colling
1.01	1012B010/00 - new FPGA; "lose of communication" [chapter 3.2.1 & 3.3.1]		Müller	Müller
1.1	1115B010/00 - new EPLD, FPGA; " System RAM changed " [chapter 3.2.1 & 3.3.1]	12.09.2001	Müller	Müller
1.2	1215B010/00 - new EPLD; "wrong byte order" [chapter 3.2.1]	20.11.2002	Müller	Müller
1.3	1220B010/02 – new FPGA; “measurement data possibly be corrupt if written as bytes”, “ETK doesn’t enter power-save mode" & “enabling the 100MBit/s calibration interface” [chapter 3.3.1]	30.06.2003	Mößner	Mößner
1.4	1220B011/02 – New Hardware State due to a quality problem with the reset components on the ETK7.1	10.11.2011	Mai	Mai

Table of Contents

1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.
Two different items are described.

- Explanation of the version-system of the ETK7.1
- The required versions of software (INCA / ASCET) , HSP (calibration hardware firmware of e.g. ES690, ES1232, MAC2...) and ETK - hardware.
  Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

2 Tool-Chain Information

2.1 Version-Syntax of the ETK7.1

The ETK7.1version information can be found on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax:

aabbcddd/ee

PLD-Code - information:
aa: EPLD-Code-Version (01, 02,... 10, 11, 12,...) see chapter 3
bb: FPGA-Code-Version (01, 02,... 10, 11, 12,...) see chapter 3

Hardware - information:
c : PCB-Version (A=V1.0, B=V1.1, C=1.2, ...)
ddd: Hardware-State of the PCB (010, 011, 012, ...) see chapter 4
ee: Assembly-Variant of the PCB (00, 01, 02, ...)

The first delivered ETK7.1 will have the version: **1011B010/00**.

2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.
If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	**Needed version**	**Remarks**
Firmware		
MAC2	V 1.123	Shipped together with the INCA software
INCA-VME-system ES1000-system	V 1.123	Shipped together with the INCA software
Software		
VS100	P4.56	
DOS ETK-Config-Tool	1.6.4	
ETK Configuration Tool	V 1.3.1	
INCA	V 2.2.3	ETK7.1 (basic mode only)
INCA	V 3.2.2	ETK7.1 (basic and compatibility mode)
ASCET SD	V4.0.14	

The registered user will automatically receive the newest INCA-version (CD-ROM)
Updates or refreshes can be downloaded from the ETAS homepage:

http://www.etas.de
http://www.etasinc.com

3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code on the ETK7.1 is stored into a programmable logic devices (EPLD and FPGA). The EPLD-code is versioned beginning with version 1.0. For the versioning syntax please refer to chapter 2.1. The FPGA-code is versioned beginning with version 1.1. For the version syntax please refer to chapter 2.1.

3.2 EPLD-Code version 1.0 is the first delivered version

3.2.1 Details of Change

Version 1.1: update file dated 08.02.2001
Error: write onto D-DPR and P-RAM not possible
Remedy: control signals were steered correctly

Version 1.2: update file dated 06.09.2002
Error: The program memory of the ETK7.1 replaces the ECU - FLASH within standard applications. Reading the code and data memory works as well as writing into the external RAM. In case of debugging the ECU code, it is possible to write into the code memory. This will become necessary e.g. in order to set break points.
In case of writing into the ETK7.1 code area the bytes will be written in wrong order (High-Byte and Low-Byte are changed).
Remedy: The control signals were steered correctly, the timing was verified

3.2.2 Delivery Conditions

This EPLD version **1.2** will be programmed into all new shipments.

3.3 FPGA-Code version 1.1 is the first delivered version

3.3.1 Details of Change

Version 1.2: update file dated 02.08.2000
Error: Under special conditions the ETK lose communication, it is necessary to reset the ETK to recover from this state.
Remedy: New FPGA - code in order to suppress this effect

Version 1.5: update file dated 07.08.2001
Cause: System RAM changed from synchronous to asynchronous

Version 2.0: update file dated 26.05.2003

Error 1: If the ECU writes measurement data as bytes and ETK reads the same address simultaneously corrupt data will possibly be read by the ETK. (If measurement data and trigger address are written in the same ECU raster this error will not occur.)

Error 2: Under special conditions the ETK does not enter the power-save mode. (behavior occurs only in a rough and noisy environment).

New feature: 16 trigger (16 measurement raster) and 100MBit/s calibration interface enabled

Remedy: New FPGA - code in order to get rid of the errors and implement the new feature.

3.3.2 Delivery Conditions

The FPGA version **2.0** will be programmed into all new shipments.

4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the part assembly of this ETK. Information about the made changes can be found below in this chapter. The hardware-state is versioned beginning with version 010. For the version syntax please refer to chapter 2.1.

4.2 Hardware-state B010 is the first delivered version

4.2.1 Details of Change

B011:

Error: Reset components from Texas Instrument (TLC7733) are causing problems, as they cannot be manufactured within the given component specification at negative temperatures any longer.

Remedy: Hardware modification of ETK-7.1 to ensure the reset is still working

4.2.2 Delivery Conditions

The hardware-state **B011** will be delivered with all new shipments.
ETKs with ‘old’ hardware-states don’t have to be be modified to the new state, as the correct function is given.

5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	**H**ardware **S**ervice **P**ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	**M**easurement & **C**alibration
RP	**R**apid **P**rototyping
PLD	**P**rogrammable **L**ogic **D**evice
FPGA	**F**ree **P**rogrammable **G**ate **A**rray; interface component to the application hardware
PCB	**P**rinted **C**ircuit **B**oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select