ETAS Entwicklungs– und
Applikationswerkzeuge
für elektronische Systeme
GmbH & Co.KG

ETK8.2

Data Sheet R1.1

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Document QH110407 R1.1

Contents

1 Overview

The ETK8.2 is a 16-bit emulator probe for 3,3 V and 5 V systems. It is compatible with earlier ETKs through the application system interface. Therefore, earlier application systems such as MAC or INCA-VME can still be used. New developments in the ES1000 (ES1232-A board) and compact (ES690) field will provide a massive increase in capability regarding the transfer rates to the calibration and development system. The ETK8.2 is set up for this expansion. Comprehensive configuration options enable the use of the ETK8.2 in connection with a variety of 16-bit processors.

ETK8.2 features:

- applicable for 16-bit microcontroller buses
- supports 16- and 8-bit access
- configurable for various microcontroller types
- usable in 3.3 V and 5 V systems
- emulation memory access time: ca. 40 to 50 ns
- two pages available, each with 128 kByte DPR emulation memory
- emulation memory configurable in 32 kByte steps
- 64 kByte measured data memory, configurable in 32 kByte steps
- permanent storage of emulation data in FLASH memory
- serial interface with 8 MBit/s or 100 MBit/s for application system
- permanent storage of configuration in E²PROM
- updates (programming of logic devices EPLD and FPGA) through software; removal of ETK or ECU not necessary.
- high flexibility
- mounting possibilities in or on ECU
- power supply: 4.3 to 18 V DC
- temperature range: - 40 ... + 110 °C
- dimensions: 94 x 54 x 12 mm

2 Function of ETK8.2

The ETK8.2 can emulate areas of an ECU program memory through Dual Port RAMs (DPRs). Figure 2-1 "ETK8.2 Architecture" shows the block-diagram. The ETK8.2 is connected to the bus of the ECU via the ECU-interface. To make this connection, an adapter is needed. A 60-pin connector contains all bus- and control signals, including connections for the power supply.

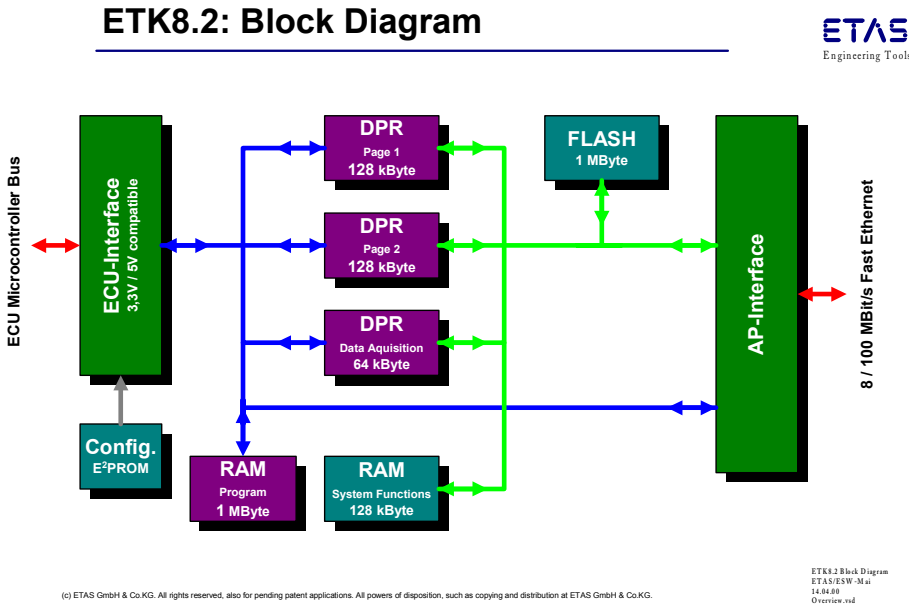


Figure 2-1 ETK8.2 Architecture

The individual blocks in this drawing will be described in detail in the following chapters.

The ECU-interface can be configured for a wide variety of applications and processors. A specific configuration is created using the "ETK-Configuration-Tool" software package. The configuration is stored in the configuration E²PROM, to set up the ETK for a specific ECU project.

While the ECU processor accesses the program data of the DPRs, the content of the DPRs can simultaneously be modified through the serial ETK-interface of the application system. This process makes adjustments of parameters, characteristic lines and maps through the application system possible. Using an additional DPR, the ECU processor can send data to the application system which receives, buffers and processes these measured data. A Flash memory is used for permanent storage of the ECU program and the adjusted parameters.

The 8 MBit/s or 100 MBit/s serial interface provides communication with the application system.

The ETK8.2 uses a 3 V/5 V mixed technology. Power supply is provided by two switching power supplies, to minimize power dissipation. Power dissipation can occur while battery voltage is converted into the voltage required by the ETK.

3 ETK8.2 Function Blocks

In this chapter, the individual function blocks are explained in detail.

3.1 ECU Interface

An ETK adapter in combination with a 60-pin connector provides connection of the ETK to the ECU. Various adapters in flexible-foil-technology are available. All bus signals (address-, data- and control bus) from the ECU are connected to the ETK8.2. A more detailed description of the connector assignment follows in chapter 4 on page 16.

The ECU interface can be flexibly configured for various applications:

- 16-bit bus, separately adjustable for read and write access
- configuration of write signals
- ...

At this point, a description of all configuration options with corresponding timing parameters would be too complex. Therefore, a configuration program ("ETK-Configuration-Tool") supports the user through a graphical interface. For a more detailed description, see section 3.6 on page 13.

3.2 Emulation Memory

The ETK8.2 is designed for communication with both conventional microcontroller systems and modern single chip systems. The ECU program can either be stored in the ETK8.2 program memory or executed from the ECU memory while only data ranges are emulated in the ETK8.2. These data ranges are stored in a Dual Port Ram (DPR) in order to enable data modification during normal ECU operation. A 1 MByte Flash memory is available for permanent storage of program code and emulation data.

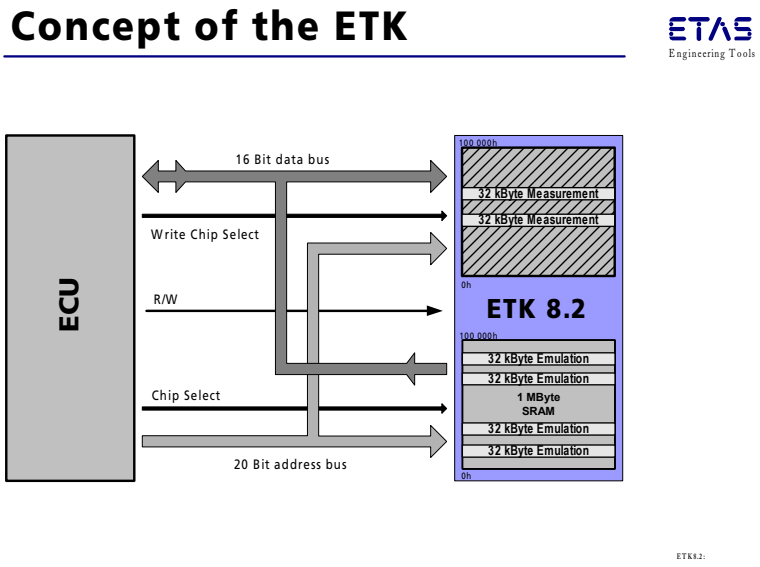


Figure 3-1 Arrangement of ECU and ETK8.2 Flash memory

The ETK8.2 has configuration options for allocating emulation memory according to specific requirements. The complete emulation memory consists of Dual Port RAMs which are divided into two 128 kByte pages (4 blocks, each 32 kByte, per page). Figure 3-2 "Emulation memory configuration: 4x 32 kByte blocks" illustrates the DPR memory configuration.

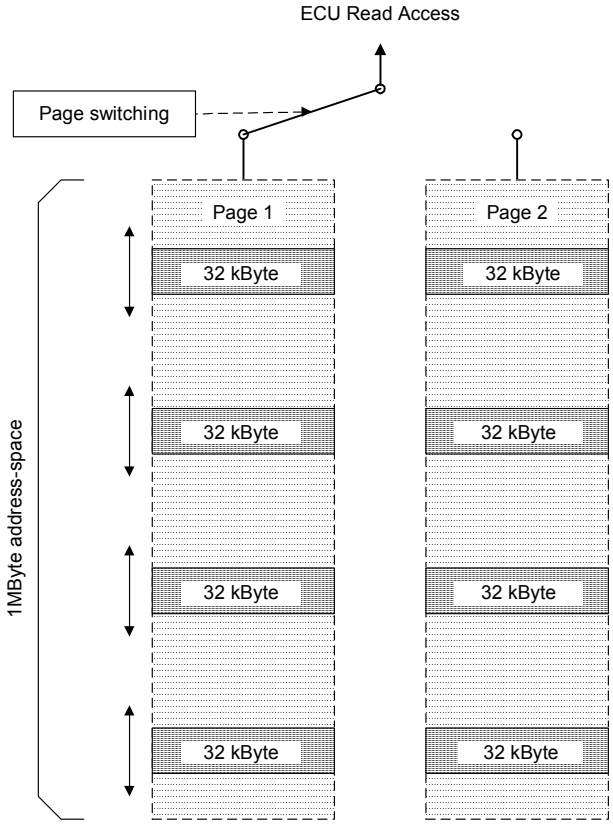


Figure 3-2 Emulation memory configuration: 4x 32 kByte blocks

Reference data can be stored on one page ("Reference page") while the data on the other page ("Working page") can be modified. It is possible to switch between the two pages during operation through the application software.

The 32 kByte blocks can be relocated in a 1 MByte (maximum) address space at 32 kByte limits.

Typically, the DPR blocks must cover the complete program data of an ECU. As the allocation depends on the respective software version of the ECU, a project-specific configuration of the ETK is necessary (see section 3.6 on page 13).

Figure 3-3 "System with external memory and ETK8.2", shows a complete overview of a system with "on chip" Flash memory, external Flash memory, "on chip" RAM and external RAM.

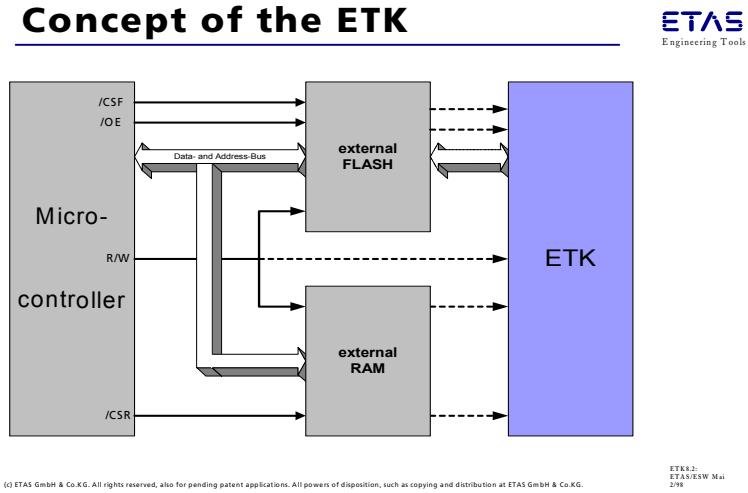


Figure 3-3 System with external memory and ETK8.2

3.2.1 Data Retention in Emulation Memory

The emulation memory physically consists of static Dual Port RAMs (DPRs) and is permanently supplied with power from the vehicle battery, to guarantee that data is preserved even when the ignition is switched off. If the ECU with ETK is isolated from the battery, the data will be lost. For brief power interruptions, e.g. during a cold start procedure, buffering through capacitors is guaranteed for several milliseconds.

3.3 Data Flash Memory

Flash memory is provided on the ETK8.2 for permanent storage of emulation data. Users can copy the contents of the emulation memory into the flash memory with the aid of the operating software. It is recommended that an updated data set is always stored in the flash memory.

The ETK8.2 has a circuit which recognizes and stores power failures. If it determines that a longer power failure has occurred and therefore, the consistency of the emulation data can no longer be guaranteed, the ETK controller initiates a copying procedure Flash memory →DPR upon restart. The Flash memory data is copied to both emulation pages. A green LED on the ETK displays the procedure. The application software announces the procedure through a message in the status line.

3.4 Code Flash Memory

Program code can also be executed from the ETK8.2 and stored in the ETK8.2 Flash memory. Storing and recalling of program code is done simultaneously to storing and recalling emulation data.

3.5 Measured Data Memory

The measured data memory is a static Dual Port RAM. Its size is 64 kByte (2 x 32 kByte blocks). The 32 kByte blocks can be relocated independently of each other in an address space of 1 MByte at 32 kByte limits. (Figure 3-4 "Measured data memory: 2 x 32 kByte blocks").

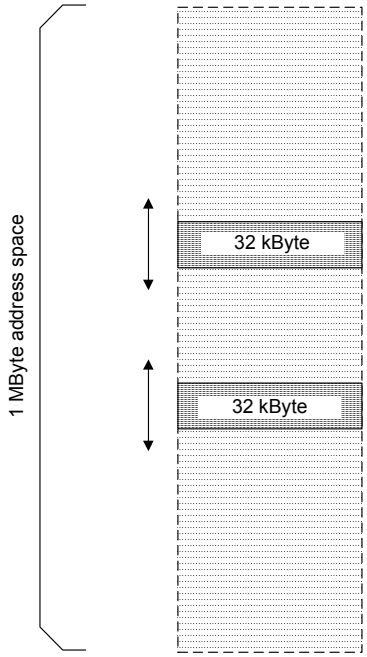


Figure 3-4 Measured data memory: 2 x 32 kByte blocks

Typically, the measured data DPR is laid over the external RAM of the ECU like a "shadow memory". The write-access of the ECU controller reaches the external RAM and the measured data DPR at the same time. The measured data stored here can be transferred to the application system via the serial ETK interface.

In addition, the measured data memory is addressed through its own chip select signal /SGWCS. Using the "ETK-Configuration-Tool", controlling of the measured data memory can be configured project-specifically (see section 3.6 on page 13).

3.5.1 Triggering of Measured Data Capture

The exact procedure for capturing measured data is explained in other documentation on Display Tables 12 and 13; only the hardware-specific features are mentioned here. The ETK8.2 contains a programmable trigger comparator which selects a segment of 64 Byte out of the 1 MByte address space. The 64 Byte segment is used for 16-bit access. This segment can be at a 64 Byte limit within the 1 MByte address space. This limit is known as the trigger segment address. Figure 3-5 "64 Byte trigger segment in the 1 MByte address space" shows the configuration of the 64 Byte trigger segment.

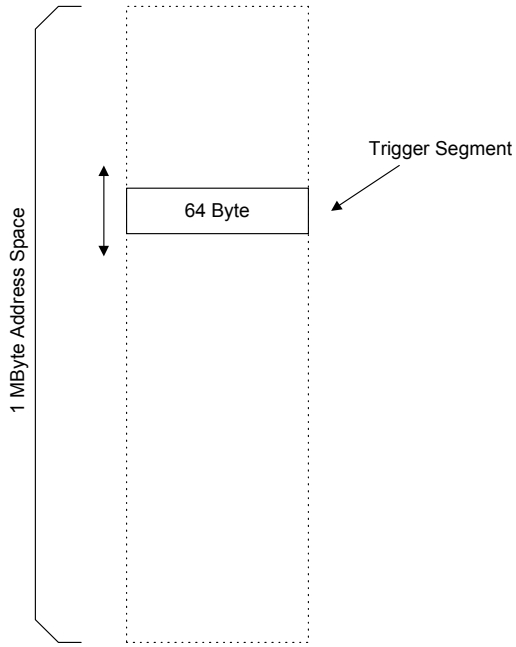


Figure 3-5 64 Byte trigger segment in the 1 MByte address space

The trigger segment address must be located in the same area as the measured data DPR (in one of the two 32 kByte blocks). If the write-protection for the emulation memory is deactivated, (TRIGSEGAD) data in unfavorable locations in the emulation memory can be changed. The "ETK-Configuration-Tool" checks this and displays an error message. Figure 3-6 "Division of the 64 Byte trigger segment" shows the address map of the 16 triggers in the 64 Byte trigger segment.

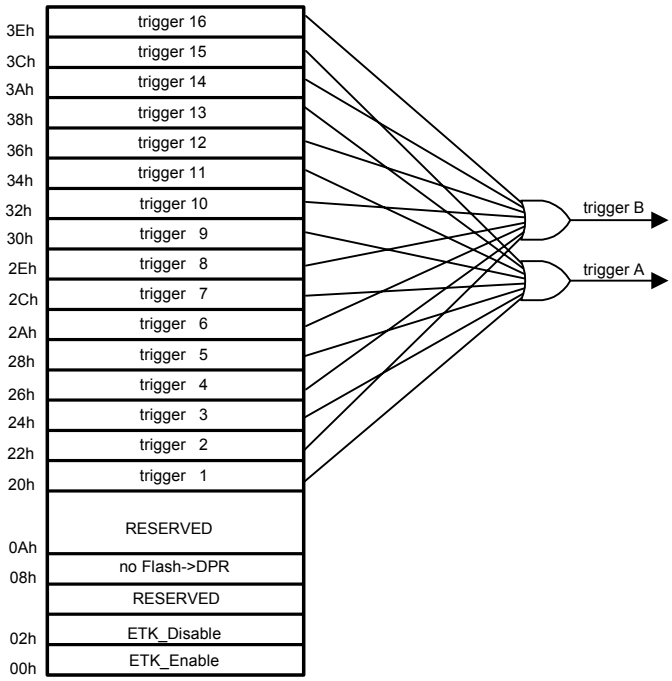


Figure 3-6 Division of the 64 Byte trigger segment

Normally, there are only two trigger addresses available: trigger B and trigger A. The new VPSI-3 card for INCA-VME will support several triggers. To achieve downward compatibility, odd-numbered triggers have been put into group trigger B and the even-numbered triggers into group trigger A. In total, 16 hardware triggers will be available.

note

The unused areas are reserved for future applications and must not be used for other purposes.

3.6 ETK Configuration

As already mentioned in previous chapters, many project-specific adjustments are necessary. A manual adjustment via solder straps is not practicable with the large diversity of projects. Configuration data is stored permanently in a serial E²PROM. Generating a valid configuration data set is supported by the PC program "ETK-Configuration-Tool".

The "ETK-Configuration-Tool" contains information on all available ETKs. The user is supported through a graphical interface.

The configuration is done in two steps:

1. Generation of the special address offset for the emulation- and measured data memory.

   The position of data and code areas, measured data output areas, trigger segment addresses etc. are familiar to the ECU software developer, or can be generated automatically. If an ECU description database (ASAP, DAMOS...) with the corresponding inputs exists, these inputs can be downloaded from this database. If necessary, a plausibility check is performed.

2. Connection of the ETK to the ECU.

   The ECU hardware developer defines the connection of the ETK to the ECU. The corresponding signals usually have to be adjusted for each processor. All inputs are checked for plausibility, to make sure that a valid configuration is generated.

note

The details of which address lines are connected to the ETK are important. It is not sufficient to connect unused address lines on GND. Adjustment in the "ETK-Configuration-Tool" is essential.

The "ETK-Configuration-Tool" can create the following output:

1. Direct ETK configuration
2. Storage of the configuration in a data file
3. Creation of the respective ASAP or DAMOS input

The most important outputs are the entries for the ASAP or DAMOS file. The parameter ETK_CFG is created and contains the complete ETK configuration of the ECU interface in hex code. If this parameter is entered correctly in the corresponding ECU description file, it guarantees that every time the application system is started, the ETK is checked for the appropriate configuration. If necessary, the ETK will be configured appropriately for the corresponding project.

3.7 Power Supply

The ETK8.2 is powered directly from the vehicle battery (permanent supply). The input voltage varies between 4.3 V and 18 V (see section 4 on page 16). The ECU voltages (USG3 and USG5) are monitored by the ETK to recognize whether the ECU is switched on or off. In case of higher input voltages (e.g. HGV) an additional voltage converter is required. The necessary voltages are created through switching power supplies which minimize heat build-up. The power supply of the ECU is not affected by the ETK8.2. A special automatic switch ensures that the power supply of the ETK8.2 is automatically switched on and off.

3.8 The Serial ETK Interface

The serial ETK interface creates the link to the application device. Data of the ETK8.2 and the application device is exchanged by a switchable 8/100 MBit/s interface. The 8 MBit/s interface is downward compatible to previous ETKs. The 100 MBit/s interface is used for future high-speed applications.

4 Technical Data

4.1 Power Supply

Parameter	Symbol	Condition	Min	Type	Max	Unit
Permanent Power Supply from car battery	U_{Batt}		5.6	12	18	V
Standby Current	ISB	U_{Batt} = 12 V; ECU off; t = 20 °C		3		mA
Active Current	IC	U_{Batt} = 12 V; ECU on; t = 20 °C		190		mA
Power Supply from ECU (sense)	USG	>3.84 →ECU on; <3.51 →ECU off				V

Table 4-1 Power Supply

4.2 Test Characteristics

Parameter	Symbol	Condition	Min	Max	Unit
Reset delay 1	t_{Reset1}	U_{Batt1}=12 V USG= 0 V↑ 5 V without transferring Flash	15	35	ms
Reset delay 2	t_{Reset2}	U_{Batt1}=12 V USG= 0 V↑ 5 V with transferring Flash	180	200	ms
Reset delay 3	t_{Reset3}	U_{Batt1}=0 V↑ 12 V transfer FPGA and Flash	260	280	ms
Data Retention	t_{Buff}	U_{Batt1}=5.6 V↓0 V	25		ms

Table 4-2 Test characteristics

note

t_{Reset1}: Delay of ECU reset through ETK without transferring the Flash (U_{Batt1} present, USG will be switched on)
t_{Reset2}: Delay of ECU reset through ETK with transferring the Flash (U_{Batt1} present, transfer active, USG will be switched on)
t_{Reset3}: max. delay of ECU reset through ETK (U_{Batt1} and USG will be switched on)
t_{Buff} : Data retention at loss of power supply

4.3 The ECU Interface

4.3.1 ETK8.2-Connector pinout

Pin	Signal	Pin	Signal
1	GND	2	SGD0
3	SGD1	4	SGD2
5	SGD3	6	SGD4
7	SGD5	8	SGD6
9	SGD7	10	GND
11	SGD8	12	SGD9
13	SGD10	14	SGD11
15	SGD12	16	SGD13
17	SGD14	18	SGD15
19	GND	20	SGA0
21	SGA1	22	SGA2
23	SGA3	24	SGA4
25	SGA5	26	SGA6
27	SGA7	28	SGA8
29	SGA9	30	SGA10
31	SGA11	32	SGA12
33	SGA13	34	SGA14
35	SGA15	36	SGA16
37	SGA17	38	SGA18
39	SGA19	40	SGSIZ
41	/SGCS	42	/SGWCS
43	GND	44	/SGRW
45	/SGRD	46	/SGOEF
47	GND	48	/SGDS
49	USG	50	/SGRES
51	IS	52	Reserved
53	GND	54	Reserved
55	Reserved	56	SGFLSHEN
57	/ETKCON	58	GND
59	SGUBATT	60	SGUBATT

Table 4-3 Connector Pinout
(Samtec Connector Ord. No.: TFM-130-02-S-D-TR)

4.3.2 Signal Description

The direction for each signal is indicated using the following abbreviations: **I**—Input Pin; **O**—Output Pin; **I/O**—Bidirectional Pin; **OD**—Open Drain Output.

Signal	Description	Dir	Pins
GND	Ground		1, 10, 19, 43, 47, 53, 58
USG	Power Supply 5 V from ECU (sense)	I	49
SGD [0 .. 15]	Data Bus: 16-bit data bus	I/O	2 - 9, 11 - 18
SGA [0 .. 19]	Address Bus: 20-bit address bus	I	20 - 39
SGSIZ	Transfer Size: together with SGA0 specifies the data transfer size (8- or 16-bit access) and the selected byte (8-bit access) for the transaction	I	40
/SGCS	Chip Select Read: Read Emulation DPR and Program Code RAM	I	41
/SGRD	Read: When asserted, indicates a read cycle. Controls output enable of ETK data bus drivers	I	45
/SGWCS	Chip Select: Write Data Acquisition DPR	I	42
/SGRES	Reset: Controls ECU System Reset	OD	50
/SGRW	Write or Write Strobe: When asserted, indicates a write cycle	I	44
/SGOEF	Controls output enable flash to ECU	O	46
/SGDS	Data Strobe	I	48
IS	Shorted to Pin 49 on ETK	O	51
SGFLSHEN	ECU Flash Program Enable	O	56
/ETKCON	3.9 k Pulldown Resistor on ETK	O	57
SGUBATT	Permanent Power Supply (5.6..18 V) from ECU	IP	59, 60
Reserved	Required for ETK8.2 (must be conn. to GND)	I	52
Reserved	Required by ETK8.2	O	54, 55

Table 4-4 Signal description

4.3.3 DC Operating Conditions—Input / Output Pins

Symbol	Parameter	Conditions	Min	Typ	Max
Input	V_{IH}	ECU=3.3 V	2		
	V_{IH}	ECU=5 V	2		
	V_{IL}	ECU=3.3 V			0.8
	V_{IL}	ECU=5 V			0.8
Output	V_{OH}	ECU=3.3 V;I_{OH}= 24 mA	2.2		
	V_{OH}	ECU=3.3 V;I_{OH}= 12 mA	2.4		
	V_{OH}	ECU=5 V;I_{OH}= 24 mA	4.3		
	V_{OL}	ECU=3.3 V;I_{OH}=24 mA			0.6
	V_{OL}	ECU=5 V;I_{OH}=12 mA			0.5

Table 4-5 DC Operating Conditions—Input / Output Pins

4.3.4 AC Operating Conditions—Microcontroller Modes

All available read and write-mode timings are displayed in the ETK Configuration Tool to facilitate the configuration of an ETK. The desired for a microcontroller can be selected from a diagram. The configuration of the ETK adjusts to match the settings in the configuration tool. The following diagrams show the read and write modes available in an ETK8.2, including the applicable timing parameter.

Mode 2: Standard Read/Write Mode

Mode 2 interprets a read/write signal additionally because the write impulse, a data strobe signal, is present during read cycles as well as during write cycles. The bus-range is evaluated through the bus size signals.

Write Cycle:

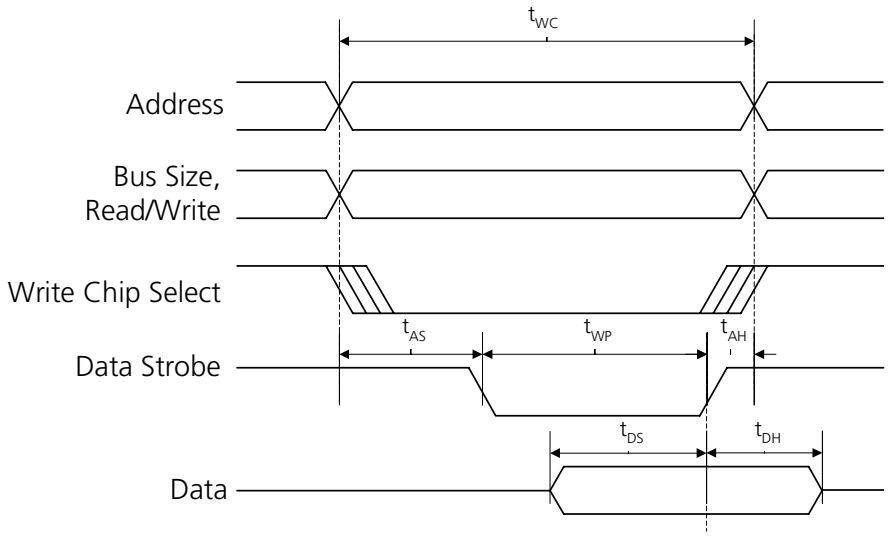
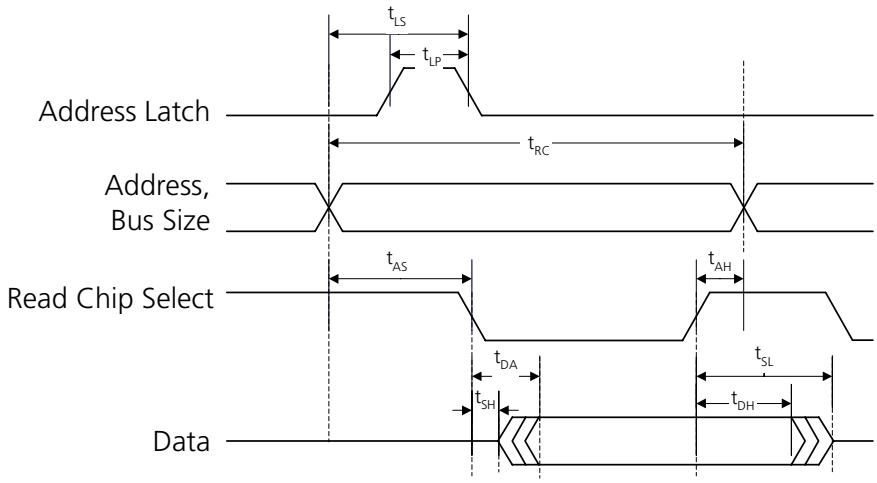


Figure 4-1 Standard Write Cycle

Symbol	Description	Min	Max	Unit
t_{WC}	Write Cycle Time	58		ns
t_{AS}	Address Setup Time	19		ns
t_{WP}	Write Pulse Width	25		ns
t_{AH}	Address Hold Time	14		ns
t_{DS}	Data Setup Time	25		ns
t_{DH}	Data Hold Time	14		ns

Read Cycle:



Address Latch: used in multiplexed mode

Figure 4-2 Standard Read Cycle

		non multiplexed		multiplexed		
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LS}	Address Latch Setup	–		7		ns
t_{LP}	Latch Pulse Width	–		5		ns
t_{RC}	Read Cycle Time	57		57		ns
t_{AS}	Address Setup Time	7		7		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DA}	Data Access Time		50		50	ns
t_{SH}	Switch On Delay	0		0		ns
t_{DH}	Data Hold Time	0		0		ns
t_{SL}	Switch Off Delay		31		31	ns

Mode 8: Fast Termination Read/Write Mode

Mode 8 uses the Chip Select and Read/Write signal for ETK access.

Write Cycle:

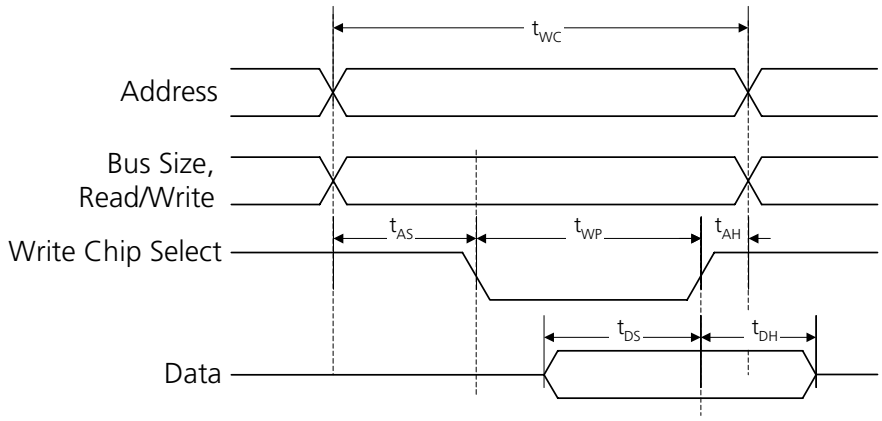
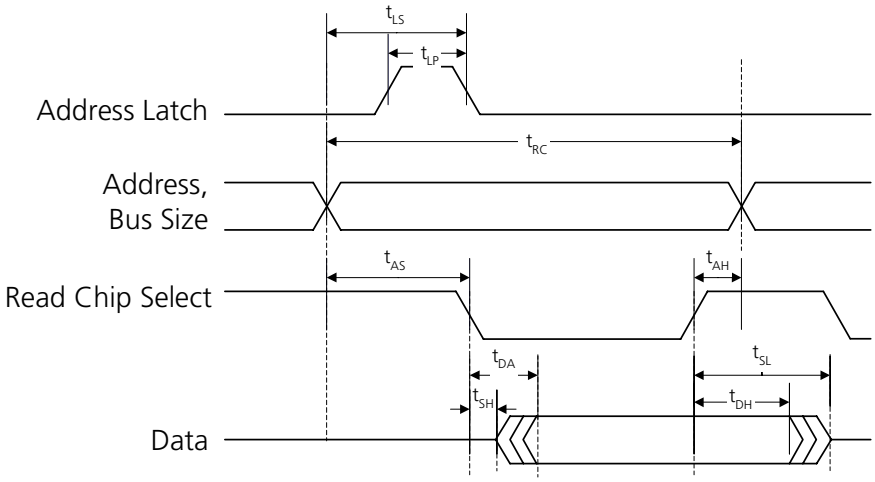


Figure 4-3 Fast Termination Write Cycle

Symbol	Description	Min	Max	Unit
t_{WC}	Write Cycle Time	53		ns
t_{AS}	Address Setup Time	19		ns
t_{WP}	Write Pulse Width	20		ns
t_{AH}	Address Hold Time	14		ns
t_{DS}	Data Setup Time	25		ns
t_{DH}	Data Hold Time	14		ns

Read Cycle:



Address Latch: used in multiplexed mode

Figure 4-4 Fast Termination Read Cycle

		non multiplexed		multiplexed		
Symbol	**Description**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{LS}	Address Latch Setup	–		7		ns
t_{LP}	Latch Pulse Width	–		5		ns
t_{RC}	Read Cycle Time	50		50		ns
t_{AS}	Address Setup Time	19		19		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DA}	Data Access Time		31		31	ns
t_{SH}	Switch On Delay	0		0		ns
t_{DH}	Data Hold Time	0		0		ns
t_{SL}	Switch Off Delay		31		31	ns

4.4 The Serial ETK Interface

4.4.1 8/100 MBit/sec Interface

The serial ETK interface utilizes a 100BASE-TX transmission to achieve an outstanding transmission performance of 100 MBit/sec. The ETK interface is also able to handle the 8 MBit/sec interface of "old" application systems. The new interface requires a new double-shielded twisted-pair cable (maximum length: 30 m).

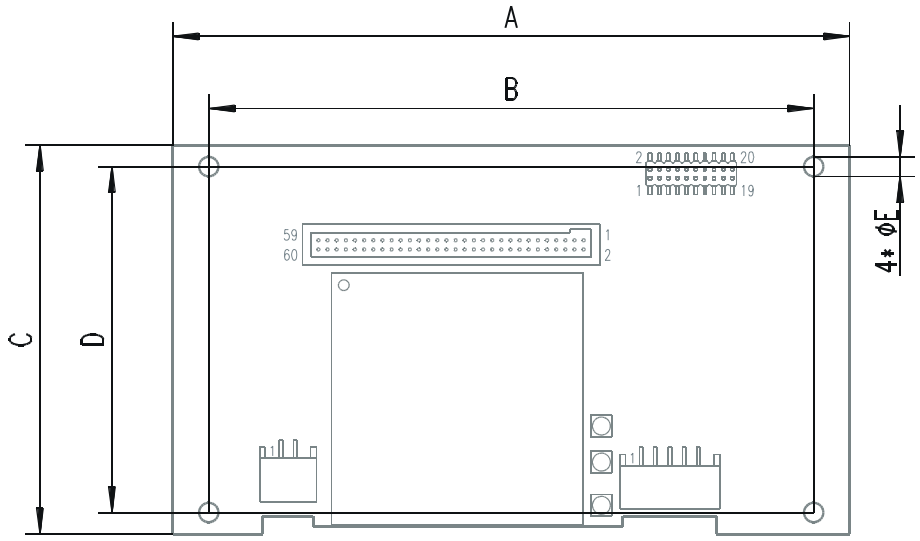
It is not possible to use the old interface cable (for 8 MBit/sec) with the new interface in the 100 MBit/sec mode. If necessary, the new interface cable can be used with the old interface.

4.5 Mechanical Dimensions and Mounting

The reference measure for all drawings is millimeter. All measures without connectors and Piggy-Backs.

4.5.1 ETK8.2 Dimensions

Dimensions	Millimeters	Inches
Length	94.0	3.701
Width	54.0	2.126
Thickness of PCB	1.7	0.067
Height of component (upper side)	5.8	0.228
Height of component (lower side)	2.20	0.087



Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	94.00	3.701	**D**	48.00	1.890
B	84.00	3.307	**E**	2.70	0.106
C	54.00	2.126			

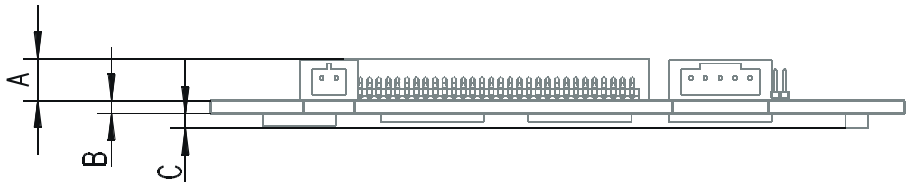


Figure 4-5 Mechanical Dimensions

Dim	Millimeters	Inches
A	5.80	0.228
B	1.70	0.067
C	2.20	0.087

4.5.2 Mounting Interface Cables

Interface Cable KA41 for Insert Socket, Proposal 1

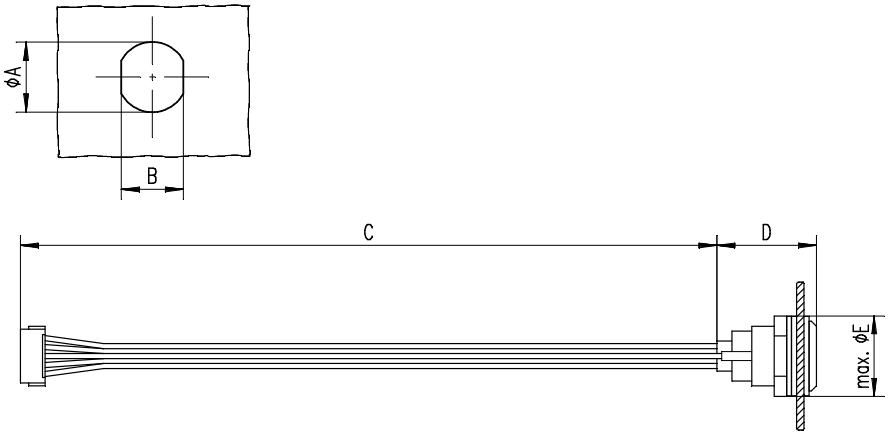


Figure 4-6 Measurement Drawing—Interface Cable KA41, Prop. 1

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	13.90	0.547	**D**	20.00	0.787
B	12.30	0.484	**E**	16.20	0.636
C	140.00	5.512			

note

Shield not connected to ECU housing.

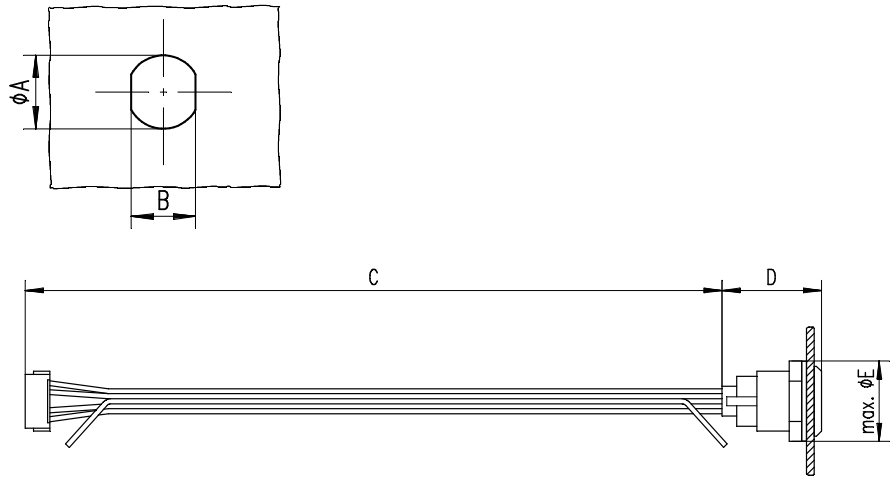


Figure 4-7 Measurement Drawing—Interface Cable KA41, Prop. 2

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	12.10	0.476	**D**	20.00	0.787
B	10.60	0.417	**E**	16.20	0.636
C	140.00	5.512			

note

Shield connected to ECU housing. Insulating disc must be removed.

note

The screws for mounting cables KA54 are not included in the KA54 delivery. They need to be ordered separately. For screw manufacturers and order numbers refer to the description of the cables.

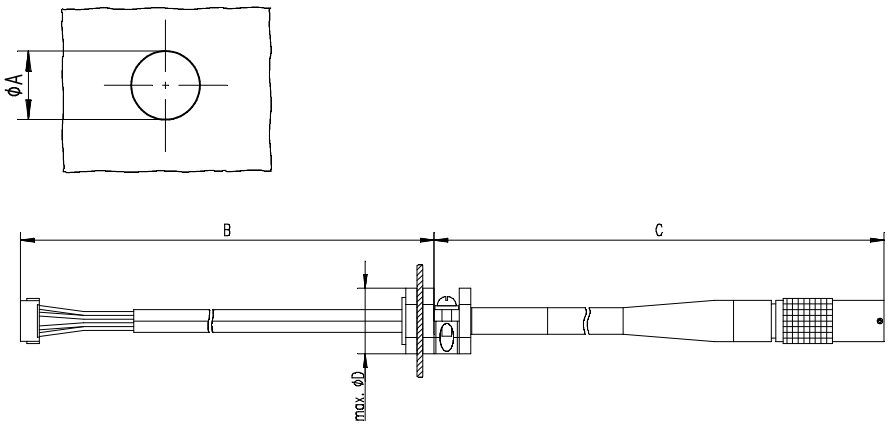


Fig. 4-8 Interface Cable KA54, Prop. 1

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	12.50	0.492	**C**	400.00	15.748
B	160.00	6.299	**D**	19.00	0.748

note

Shield connected to ECU housing.

SKINDICHT *compact screwing;* ***Manufacturer****: Lapp;* ***Description****: SH7;* ***Order-No.****: 5200 0830*

Nut for compact screwing; ***Manufacturer:*** *Lapp;* ***Description:*** *SM7;*
Order-No.: *5200 3490*

note

The screws for mounting cables KA54 are not included in the KA54 delivery. They need to be ordered separately. For screw manufacturers and order numbers refer to the description of the cables.

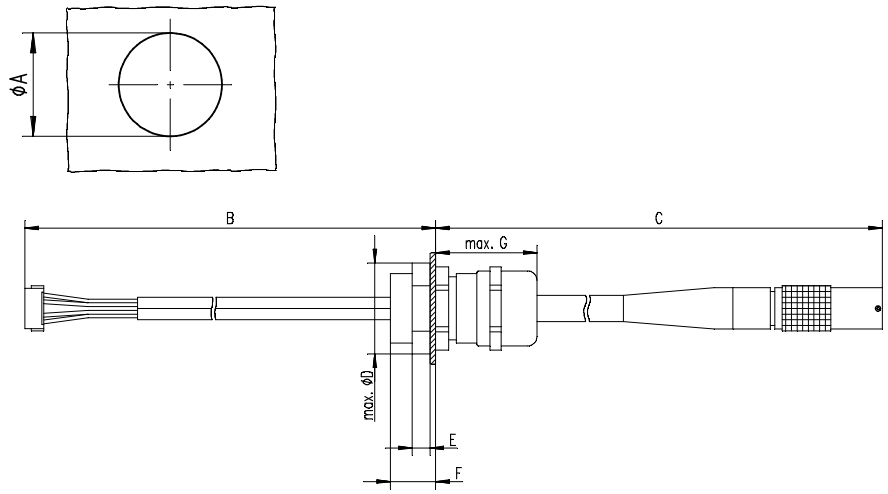


Fig. 4-9 Interface Cable KA54, Prop. 2 (long thread)

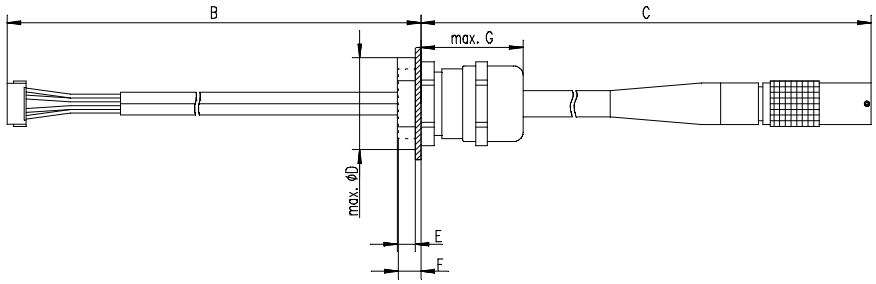


Fig. 4-10 Interface Cable KA54, Prop. 2 (short thread)

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	18.80	0.740	**E**	4.70	0.185
B	160.00	6.299	$\mathbf{F}_{Long}$	12.00	0.472
C	400.00	15.748	$\mathbf{F}_{Short}$	6.00	0.263
D	24.25	0.955	**G**	27.00	1.063

note

Shield connected to ECU housing.

SKINTOP *compact screwing;* ***Manufacturer:*** *Lapp;* ***Description:*** *MS-SC 11 ;* ***Order-No.:*** *5311 2320 (long thread) or 5311 2220 (short thread)*

Nut for compact screwing; ***Manufacturer:*** *Lapp;* ***Description:*** *SM-PE 11 ;* ***Order-No.:*** *5210 3220*

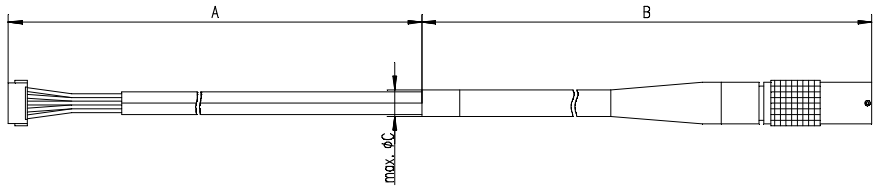


Figure 4-11 Measurement Drawing—Interface Cable KA40

Dim	Millimeters	Inches
A	160.00	6.299
B	400.00	15.748
C	7.50	0.295

note

Strain relief on ECU cover necessary. Shield not connected to ECU housing.

4.5.3 Mounting Power Supply Cables

Cable ETV

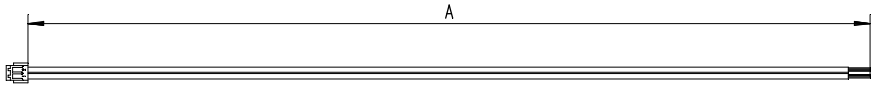


Figure 4-12 Power Supply Cable ETV

Dim	Millimeters	Inches
A	190.00	7.480

Cable with Filtercoil ETV2

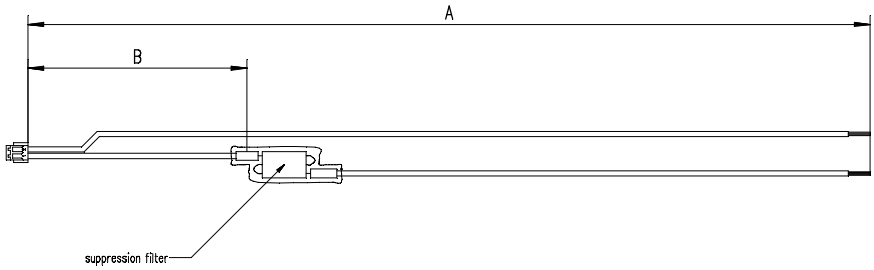


Figure 4-13 Power Supply Cable with Filtercoil ETV2

Dim	Millimeters	Inches
A	190.00	7.480
B	50.00	1.969

Cable Adapter KA43

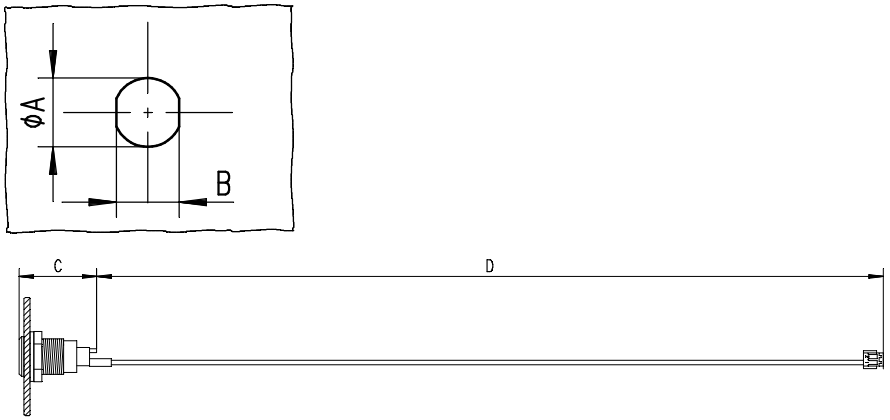


Figure 4-14 Cable Adapter KA43

Dim	Millimeters	Inches
A	190.00	7.480
B	8.30	0.327
C	19.50	0.768
D	200.00	7.874

Cable Adapter with Filtercoil KA50

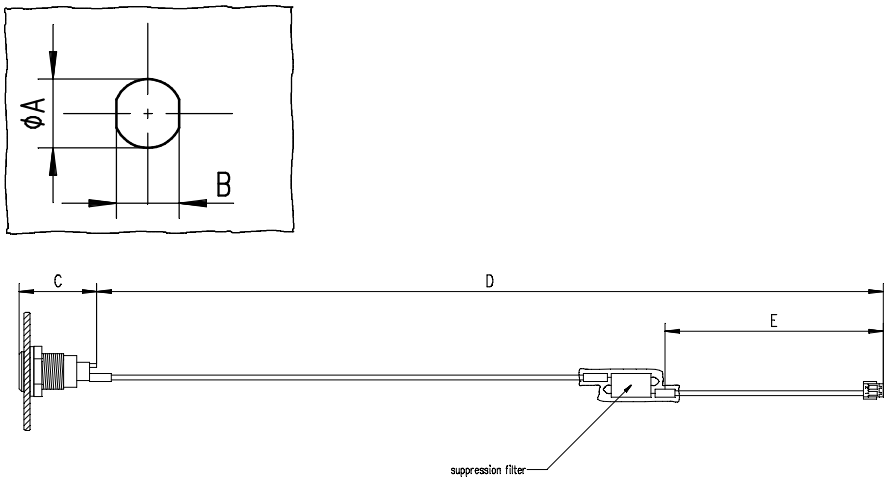


Figure 4-15 Cable Adapter with Filtercoil KA50

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	190.00	7.480	**D**	200.00	7.874
B	8.30	0.327	**E**	50.00	1.969
C	19.50	0.769			

5 ETK Configuration

In this chapter, the configuration parameters of the ETK8.2 will be described. The configuration is possible through the ETK Configuration Tool. Not all combinations of parameters make sense and at this point, not all possible configurations are implemented. The Configuration Tool provides support concerning the configuration parameters. The following is a list with configuration parameters:

- Format (Intel/Siemens/Motorola)

  The selection of the processor type defines, which bit of the data or address lines is the most significant bit (MSB) respectively the least significant bit (LSB). This definition determines how the connection of the address and data lines has to be made.

- Read Bus Width (8 Bit, 16 Bit)

  Data Bus width during read access to the ETK8.2 using the /SGCS Chip Select Signal.

- Read Bus Mode (Multiplex, Non Multiplex)

  During multiplexed operation, the address and data information on the data Bus SGD[] are transmitted one after the other. The address information in the ETK8.2 are latched by using the SGALE signal.

- Write Bus Width (8Bit, 16 Bit)

  Data Bus Width during write access to the ETK8.2 using the /SGWCS Chip Select Signal

- Write Bus Mode (Multiplex, Non Multiplex)

  During multiplexed operation, the address and data information on the data Bus SGD[] are transmitted one after the other. The address information in the ETK8.2 are latched by using the SGALE signal.

- Write Signal Configuration (One Write Signal, /UB /LB Write Only, /UB /LB Read/Write)

  This configuration parameter determines the connection of the write strobe signal. A write signal has to be connected to /SGRW at the first configuration possibility. Either a writing or a reading/writing signal has to be connected to SGSIZ and SGALE during the other two possibilities.

- Write /CS (Without /SGWCS, with /SGWCS)

  This parameter determines, if a write access happens with or without writing Chip Select (/SGWCS). For internal timing reasons, a write access with Chip Select is to be preferred.

- Code/Data Memory (Write Protected, Write Enabled)

  Write protection for the code and data emulation memory (/SGCS)

- DPR Access (Normal, Ignore A16 .. A19)

  If using the normal configuration, all address lines are decoded during a write access to the measured data memory. Otherwise the lines SGA[16..19] will be ignored.

6 Order Information

Type	Order-No.	Note
ETK8.2	F 00K 001 799	
Interface Cables:		
KA41, Prop. 1 / Prop. 2	Y 261 A24 729	
KA54, Prop. 1 / Prop. 2	F 00K 001 302	Delivery without PG-screwing
KA40	Y 261 A24 736	
Power Supply Cables:		
ETV	Y 261 A24 446	
ETV2	F 00K 000 593	
KA43	Y 261 A24 941	
KA50	F 00K 000 940	

Figures