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Comments :	Currently shipped: 24E013 FPGA-Code version: V2.4 Hardware-state: E013			
Created:	Name Mai	Department ETAS / PHW-EES1	Signature Mai	Date 24.04.2008
Checked:	Name Meerwein	Department ETAS / PHW-EES21	Signature Meerwein	Date 24.04.2008

C h a n g e s

Revision	Description	Date	Name	Signature
1.0	11B011 - initial version (reset generator integrated)	08.08.2001	Colling	Colling
1.1	11B012 - pull up resistor at MDA31-port removed	25.10.2001	Müller	Müller
1.2	12B012 - new FPGA version - wrong measure data possible because of faulty DPR structure	12.12.2001	Müller	Müller
1.3	13B012 - new FPGA version - because of RAM lot problems	06.05.2002	Müller	Müller
1.4	20B013 - new product variant, enabling the 100MBit/s calibration interface and new coil for power supply	13.11.2002	Müller	Müller
2.1	23E013 - HW redesign due to discontinuation of some components	09.05.2007	Mai	Mai
2.2	24E013 – new FPGA version – measurement problem due to wrong trigger segment address decoding	24.04.2008	Mai	Mai

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1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the necessary tool-chain to use this ETK.

Two different items are described.

- Explanation of the version syntax of the ETKP4.0-x
- The necessary software-, firmware- and hardware-versions or other requirements of the used tool-chain components so that the ETK is working.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

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2 Tool-Chain Information

2.1 Version-Syntax of the ETKP4.0-x

The ETKP4.0-x version information can be found on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: **aacddd/ee**

PLD-Code information:

aa: FPGA-Code-Version (10, 11, 12,...) see chapter 3

Hardware information:

c : PCB-Version (A, B, C, ...)
ddd: Hardware-State of the PCB (010, 011, 012, ...) see chapter 4
ee: Assembly-Variant of the PCB (00, 01, 02, ...)

The first delivered ETKP4.0 hardware state was **11B011/00**.

Customer variants of this ETK will be additionally differentiated using different letters in the name (ETKP4.0-A, ETKP4.0-B, ...) and different order numbers (F-00K-...).

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2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.

If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
Firmware		
MAC2	V 4.3	Shipped together with the INCA software
INCA-VME-system ES1000-system	V 4.9	Shipped together with the INCA software
Software		
VS100	Not supported	
DOS ETK-Config-Tool	Not supported	
ETK Configuration Tool	V 1.4.1	
INCA	V 3.1.0	ETKP4.0-x (basic mode only)
INCA	V 3.2.2	ETKP4.0-x (basic and compatibility mode)
INCA	V 4.0.0	ETKP4.0-x (basic, compatibility and advanced mode)

The registered user will automatically receive the newest INCA-version (CD-ROM)

Updates or refreshes can be downloaded from the ETAS homepage:

<http://de.etasgroup.com>

<http://en.etasgroup.com>

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3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETKP4.0 is stored onto a programmable logic devices (PLD). The PLD-code starts with version 1.1. For the version syntax please refer to chapter 2.1.

3.2 PLD-Code version 1.1 was the first delivered version

3.2.1 Details of Change

Version 1.1: update file dated 08.08.2001

Version 1.2: update file dated 12.11.2001

Error: Currently none, but DPR read problem observed with ETKP5 may replicate here, since ETKP4 and ETKP5 use the same DPR.

Remedy: New FPGA code with modified DPR read timing as a preventive action to avoid possible DPR read problems in the future.

Cause: Invalid data read from DPR under certain timing conditions due to the self-clocked internally synchronous architecture of the otherwise asynchronous memory.

Version 1.3: update file dated 03.05.2002

Error: During flash programming at low temperature, data corruption may occur sporadically.

Remedy: Timing in FPGA changed

Version 2.0: update file dated 21.10.2002

Cause: 16 trigger (16 measurement raster) and 100MBit/s calibration interface enabled

Precondition: The hardware state B013 is required for updating the PLD code version 2.0 .

Version 2.3: update file dated 25.04.2007

Cause: As some components of the ETKP4 HW Revision B are discontinued, a new FPGA code is needed

Hint: This new HDC is only valid for the HW Revision E

Version 2.4: update file dated 21.04.2008

Error: Measurement with ETK will not work, when using trigger segment address ending with 0x40 or 0xC0.

Remedy: Trigger segment address decoding in FPGA changed

Hint: This new HDC is only valid for the HW Revision E

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Attention: The ETK HDC update is performed with the ETK Configuration Tool. The update process must not be interrupted and will take some minutes.

3.2.2 Delivery Condition

The PLD version **2.4** will be programmed into all new shipments.

4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes are listed underneath. The hardware-state starts with version B011. For the version syntax please refer to chapter 2.1.

4.2 Changes from Hardware-state B011 to version B012

4.2.1 Details of Change

Changes:

- R208 removed upon request of RB/DS; ETK identification won't be done about MDA31 and pull up resistor in general at RB/DS

4.3 Changes from Hardware-state B012 to version B013

4.3.1 Details of Change

Changes:

- Improved L800 (MP2+) with higher saturation current

4.4 Changes from Hardware-state B013 to version E013

4.4.1 Details of Change

Changes:

- HW had to be redesigned due to obsolete components. The electrical characteristics remained the same!

4.4.2 Delivery Condition

The hardware-state **E013** will be delivered with all new shipments.

B-Revision ETKP4 can be modified to the latest B-Revision states, but can not be upgraded to the E-Revision!

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4.5 Assembly-Variant

Assembly-Variant		
Rev.	Variant	Description
B	00	ETKP4.0-K (Oak on socket),
	01	ETKP4.0-A (MPC561/562 soldered on board), (CS2)
	02	ETKP4.0-B (MPC563/564 soldered on board), (CS2)
E	01	ETKP4.0-K (Oak on socket),
	02	ETKP4.0-A (MPC561/562 soldered on board), (CS2)
	03	ETKP4.0-B (MPC563/564 soldered on board), (CS2)

5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	H ardware S ervice P ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	M easurement & C alibration
RP	R apid P rototyping
PLD	P rogrammable L ogic D evice
FPGA	F ree P rogrammable G ate A rray; interface component to the application hardware
PCB	P rinted C ircuit B oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select