ETAS

ETKP5.0
Emulator Probe for MPC555

Data Sheet

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Contents

1 Overview

The ETKP5.0 is an emulator probe especially for the Motorola PowerPC MPC555 processor (abbreviated MPC). It is compatible with earlier ETKs through the calibration and development system interface. Therefore, earlier calibration and development systems such as MAC or ES1000.1 can be used. In the future, new developments in the ES1000.2 (ES1231 board) and the compact module field (ES690) will provide a massive increase in capability regarding the transfer rates to the calibration and development system. The ETKP5.0 is set up for this expansion.

ETKP5.0 features:

- applicable for an external MPC 16-bit microcontroller bus

- supports 16- and 8-bit access to the data emulation memory

- usable in 3.3 V systems (5 V tolerant data bus)

- two pages of data emulation/measurement data memory available, each with 256 kByte

- memory access time: max. 1 WS / 40 MHz

- permanent storage of emulation data in FLASH memory

- serial interface with 8/100 MBit/s to the calibration and development system

- permanent storage of configuration in E²PROM

- firmware update (programming of the logic device) through software; removal of ETK or ECU not necessary.

- power supply: 4.3 to 18 V DC

- temperature range: -40 ... +110 °C

- dimensions: ca. 61 x 64 x 10 mm

2 Function of ETKP5.0

Fig. 2-1 "ETKP5.0 Architecture" shows the blockdiagram of the ETKP5.0. The processor is directly soldered on the ETKP5.0 so that no additional adapter is needed. The connection to the ECU is made by an BGA connector. The processor can read directly from one of the two pages of the data emulation memory and can write its data directly to the measurement data memory. These two memories (data emulation memory, measurement data memory) are using the same address space and are realized inside the same DPRs. Through the BGA connector the processor can communicate with other external memories or peripheral components too. All processor signals are accessible on the BGA connector.
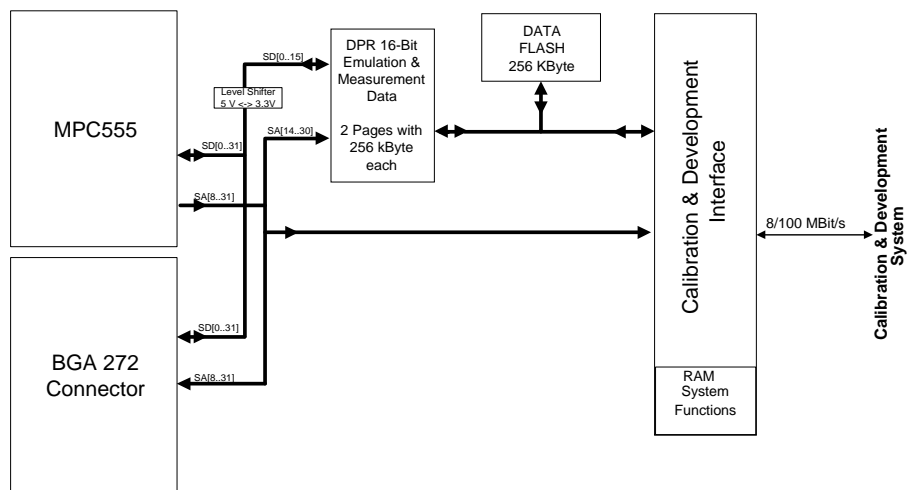

Fig. 2-1   ETKP5.0 Architecture

While the processor accesses the program data (not the program code) out of the data emulation memory, the content of the data emulation memory can simultaneously be modified by the calibration and development system through the serial ETK-interface. This process enables adjustments of parameters, characteristic lines and maps through the calibration and development system. Using an additional measurement data memory area, the ECU processor can send data to the calibration and development system which receives, buffers and processes this measured data. A flash memory is available for permanent storage of the adjusted parameters (program data).

The 8/100 MBit/s serial interface provides communication with the calibration and development system.

The ETKP5.0 uses a 3.3 V technology. The power supply for the ETKP5.0 is provided by a switching power supply, to minimize power dissipation.

3 ETKP5.0 Function Blocks

In this chapter, the individual function blocks of the ETKP5.0 are explained in detail.

3.1 Processor Interface

The entire processor interface to the calibration and development system memories has a 16-bit-wide data bus and uses only one chip select for read and write accesses.

The processor can read and write its data directly from or to the data emulation and measurement data memory. Fig. 3-1 "System with internal and external memory" shows an overview of the system with "on chip" Flash and RAM and external Flash and RAM memory. It also shows the possibilities to access the different memories with its chip selects. The chip select of the data emulation and measurement data memory can be chosen (/CS0, /CS3) by soldering the respective bridge on the PCB (default is /CS0, see 3.10 "Chip Select Configuration Bridge").
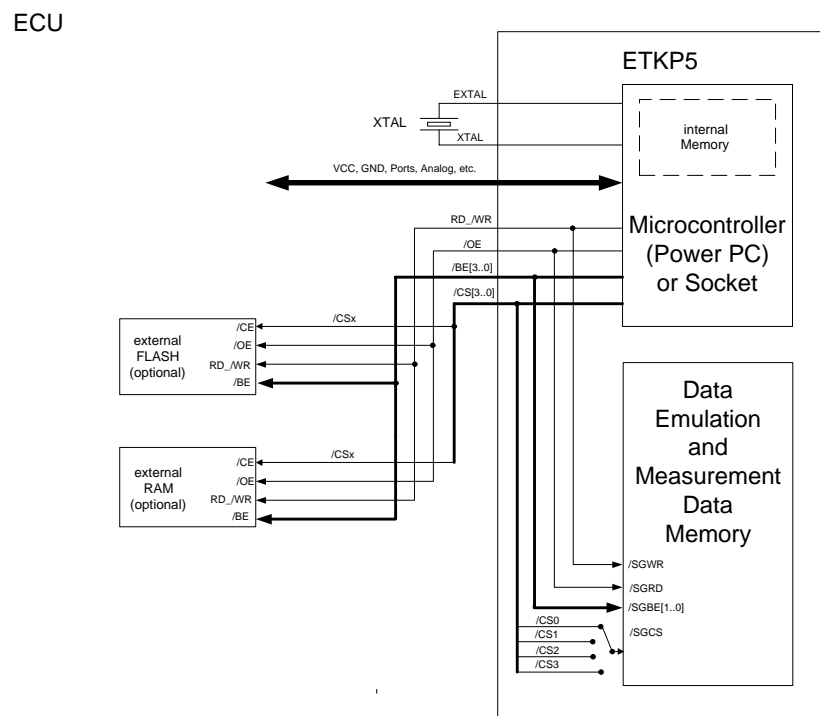

Fig. 3-1   System with internal and external memory

3.2 BGA Connector

The BGA connector interfaces the processor with the ECU. All signals of the processor are directly connected to the BGA connector. Also the clock signal must be provided through the connector to the MPC.

3.3 Data Emulation and Measurement Data Memory

The complete data emulation and measurement data memory consists of two 256 kByte pages (Fig. 3-2 "Data Emulation and Measurement Data Memory: 2 Pages with 256 kByte each"). The address range of the used chip select to address the data emulation and measurement memory must be 256 kByte and it must be defined at a 256 kByte limit.

The size and offset address of the measurement data memory is variable. It is laid inside the 256 kByte address range of the data emulation and measurement data memory.

3.3.1 Data Emulation Memory

During operation of an ECU, only program data, not program code, can be modified by using the data emulation memory. Modification of program code would inevitably lead to a system crash. The program code is continuously processed out of the internal or external memory. Motorola PowerPC controllers support this concept.
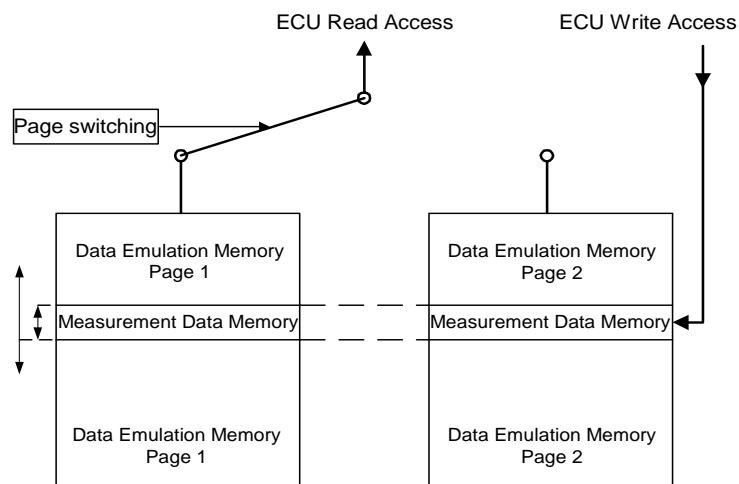

Fig. 3-2 Data Emulation and Measurement Data Memory: 2 Pages with 256 kByte each

Reference data can be stored on one page ("Reference page") while the data on the other page ("Working page") can be modified. It is possible to switch between the two pages during operation through the application software.

3.3.2 Measurement Data Memory

The measurement data memory must be located within the address space of the data emulation and measurement data memory. It can have variable size.

The measured data stored here can be transferred to the calibration and development system via the serial ETK interface.

> **note**
>
> *Because there is no write protection of the data emulation memory possible, it must be taken care not to override emulation data.*

3.3.3 Triggering of Measurement Data Capture

The exact procedure for capturing measured data is explained in the documentation Display Tables 12 and 13; only the hardware-specific features are mentioned here. The ETKP5.0 contains a trigger comparator which selects a segment of 64 Byte out of the measurement data memory address space (at a 64 Byte limit). This limit is known as the trigger segment address. Fig. 3-3 "Division of the 64 Byte Trigger Segment" shows the configuration of the 64 Byte trigger segment.
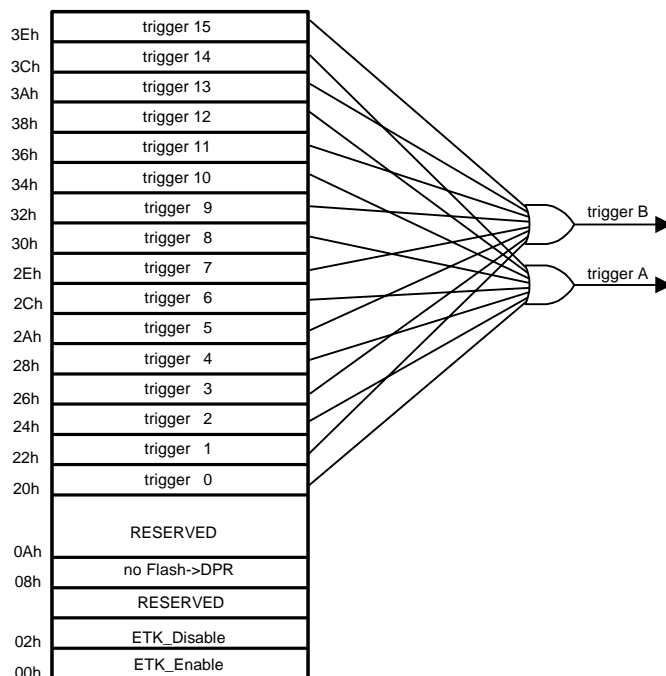
.

Fig. 3-3   Division of the 64 Byte Trigger Segment

Usually, there are only two trigger addresses available: trigger B and trigger A. The new ES1231 board for the ES1000.2 system and the new compact module ES690 will support several triggers. To achieve downward compatibility, odd-numbered triggers have been put into group trigger B and the even-numbered triggers into group trigger A. In total, 16 hardware triggers will be available.

> **note**
>
> *The unused address areas are reserved for future applications and must not be used for other purposes.*

3.3.4 Data Retention in Data Emulation Memory

The data emulation and measurement data memory physically consists of a static Dual Port RAM and is permanently supplied with power from the car battery, to guarantee that data is preserved even when the ignition is switched off. If the ECU with ETK is isolated from the battery, all data will be lost. For brief power interruptions, e.g. during a cold start procedure, buffering is guaranteed through capacitors for several milliseconds.

3.3.5 ETKP5.0 Deactivation

It can be necessary that the ETK does not respond to read or write accesses of the processor. Therefore the processor can switch off the ETKP5.0 chip select. To indicate to the calibration and development system that the processor has "switched on" or "switched off" the ETK a write access bevore switching off the ETK and after switching on the ETK to the trigger segment (see Fig. 3-3 "Division of the 64 Byte Trigger Segment") must occur.

Through writing to the address ETK_Disable (trigger segment address + 0x02h) the "switching off" will be indicated. Through writing to the address ETK_Enable (trigger segment address) the reactivation of the ETK will be indicated. The data used during the write accesses are meaningless.

> **note**
>
> *These two addresses are not protected against accidental write access. Due to the fact that they belong to the trigger segment, they are allocated in the address space of the measurement data memory.*

3.4 Data Flash Memory

Flash memory is provided on the ETKP5.0 for permanent storage of emulation data. Users can copy the contents of the data emulation and measurement data memory into the flash memory using the operating software. It is recommended that an updated data set is always stored in the flash memory.

The ETKP5.0 has a circuit which recognizes and stores power failures. If this circuit detects a longer power failure, and therefore a possible inconsistency of the emulation data, the ETK controller initiates a copying procedure Flash memory → DPR upon restart. The Flash memory data is copied to both emulation pages. A green LED on the ETK displays the procedure. The operating software announces the procedure by a message in the status line.

If the ETKP5.0 is used as a normal RAM it may be useful that this copying procedure is switched off. This can be done by doing a write cycle to a dedicated address in the trigger segment (trigger segment address + 0x08h, see Fig. 3-3 "Division of the 64 Byte Trigger Segment"). The green LED on the ETK will be switched off.

> **note**
>
> *The Flash memory on the ETKP5.0 only stores data which exists in the data emulation and measurement data memory of the ETKP5.0. The program code is stored only in the ECU Flash memory.*

3.5 Code Flash Memory

The program code is not emulated by the ETKP5.0. The program code is stored in the ECU Flash memory ("on chip" and/or external) and is not modified by the ETKP5.0. Only the accessible emulation data areas are emulated by the ETKP5.0. The ECU Flash memory can be programmed with the normal Flash memory programming tools.

3.6 ETK Configuration

As already mentioned in previous chapters, some project-specific adjustments are necessary. Configuration data is stored permanently in a serial E²PROM. Generating a valid configuration data set is supported by the "ETK Configuration Tool". The "ETK Configuration Tool" contains information on all available ETKs. The user is supported through a graphical interface.

The "ETK Configuration Tool" can create the following output:

1. Direct ETK configuration
2. Storage of the configuration in a data file
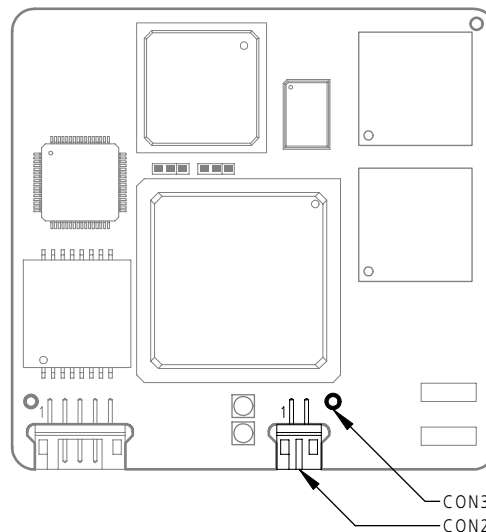
3.7 Power Supply

Fig. 3-4   Power Supply Connectors

The ETKP5.0 is powered directly from the car battery (permanent supply). The input voltage varies between 4.3 V and 18 V. The ECU voltage (USG3) is monitored by the ETK to recognize whether the ECU is switched on or off. In case of higher input voltages to the ETK an additional voltage converter is required. All necessary voltages are created through switching power supplies which minimizes heat build-up. The power supply of the ECU is not affected by the ETKP5.0. An automatic switch ensures that the power supply of the ETKP5.0 is automatically switched on and off.

The ETKP5.0 can be supplied with power through the 2-pin power supply connector (CON2: U_{Batt1} = Pin1; GND = Pin2) and additionally through CON3 a through-hole solder pad to connect a power supply U_{Batt2}. The power supply on CON3 must use the GND of CON2.

> **note**
>
> *Do not switch on the ECU while the ETK power supply is unconnected. Connect the ETK power supply first.*

3.8   The Serial ETK Interface

The serial 8/100 MBit/s ETKP5.0 interface creates the link to the calibration and development system. The ES1231 plug-in board for the ES1000 high-end VME system and the new compact module ES690 will support the 100 Mbit/s interface.
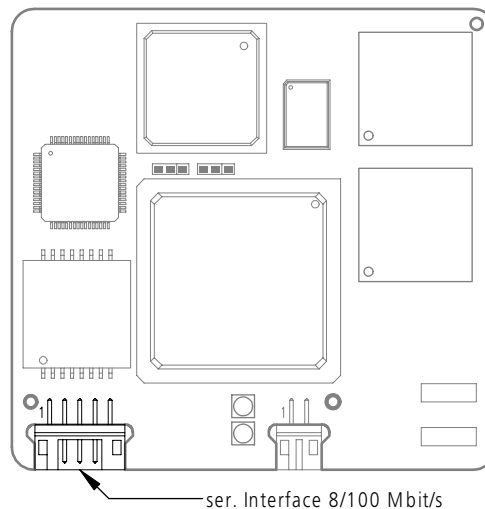

ser. Interface 8/100 Mbit/s

Fig. 3-5   Location of the Serial ETK Interface

The interface utilizes a 100BASE-TX transmission to achieve an outstanding transmission performance of 100 MBit/sec. The ETK interface is also able to handle the 8 MBit/sec interface of "old" calibration and development systems. The new interface requires a new double-shielded twisted-pair cable (maximum length: 30 m).

It is not possible to use the old interface cable (for 8 MBit/sec) with the new interface in the 100 MBit/sec mode. The new interface cable can be used with the old interface.

3.9   Status LEDs

There are two LEDs on the ETKP5.0 (ETK On: red; Flash Data: Green), displaying the operating conditions of the ETKP5.0.

The red LED turns on when the ETKP5.0 is supplied with power and either the ECU and/or the calibration and development system (MAC, ES1231 or ES690) is connected and ready to communicate with the ETKP5.0.
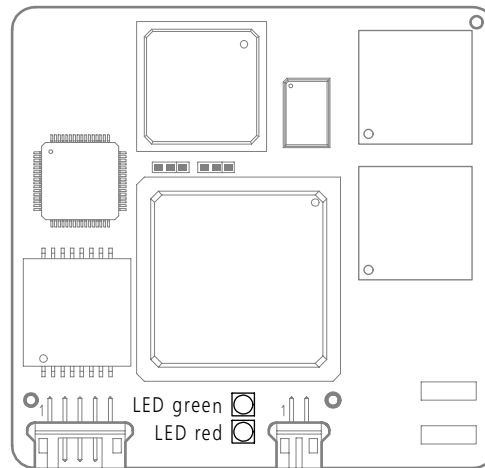

Fig. 3-6   Status LEDs

If the data retention of the DPRs is no longer ensured because of a power supply decline under 3.5 V, the green LED turns on. As soon as the ETKP5.0 switches on again, the content of the Flash will be copied into the RAMs. For continuous visibility of possible loss of data, the green LED stays on until the calibration and development system copies new data into the RAMs.

3.10   Chip Select Configuration Bridge

BR100 and BR 103 are the solder bridges for chip select configuration.

BR100	BR103	Chip Select
1-2	open	/CS0 (default)
open	1-2	/CS1
2-3	open	/CS2
open	2-3	/CS3
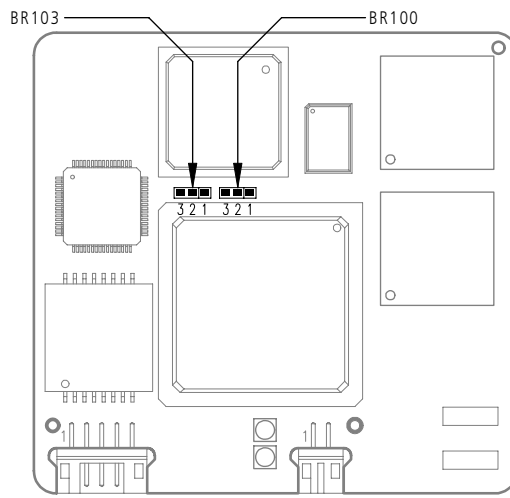
Fig. 3-7   Chip Select Configuration Bridges

4   Technical Data

4.1   Power Supply

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Permanent Power Supply from car battery	UBatt1		4.3	12	18	V
Permanent Power Supply from car battery (Standby)	UBatt1		3.5	12	18	V
Standby Current	ISTBY	UBatt1 = 12 V; ECU off; t = 20°C			30	mA
Supply Current	IBatt1	UBatt1 = 4.3 V; ECU on; t = 20°C		160	320	mA
Supply Current	IBatt1	UBatt1 = 12 V; ECU on; t = 20°C		60	90	mA
Supply Current	IBatt1	UBatt1 = 18 V; ECU on; t = 20°C		40	60	mA
Power Supply from ECU (sense)	USG3	>2.36 -> ECU on <2.21 -> ECU off		3.3		V

4.2   Testcharacteristics

Parameter	Symbol	Condition	Min	Max	Unit
Reset delay 1	t_{Reset1}	U_{Batt1}=12 V USG= 0 V↑ 3.3 V without transferring Flash	15	35	ms
Reset delay 2	t_{Reset2}	U_{Batt1}=12 V USG= 0 V↑ 3.3 V with transferring Flash	28	48	ms
Reset delay 3	t_{Reset3}	U_{Batt1}=0 V↑ 12 V transfer FPGA and Flash	228	518	ms

note

t_{Reset1}: Delay of ECU reset through ETK without transferring the Flash (U_{Batt1} present, USG will be switched on)
t_{Reset2}: Delay of ECU reset through ETK with transferring the Flash (U_{Batt1} present, transfer active, USG will be switched on)
t_{Reset3}: max. delay of ECU reset through ETK (U_{Batt1} and USG will be switched on)

4.3 Electrical Characteristics

4.3.1 3.3 V Signals

3.3 V Signals are DATA[15..0].

Type	Parameter	Conditions	Min	Max
Input	V_{IH}		2.0 V	7.0 V
	V_{IL}			0.8 V
	I_I	/HRESET inactive		20 µA
		/HRESET active		1 µA
Output*	V_{OH}	I_{OH} = -4 mA	2.2 V	
	V_{OL}	I_{OL} = 4 mA		0.4 V

Parameter	Conditions	Typ.
C_{IO}	DATA[15..0]	23.5 pF

4.3.2 3.3 V Signals

2.6 V Signals are /CS-ETK, /OE, RD_/WR, /WE_AT[1..0], /HRESET, /PORESET, ADDR[30..14].

Type	Parameter	Conditions	Min	Max
Input	V_{IH}		2.2 V	3.8 V
	V_{IL}			0.8 V

Parameter	Conditions	Typ.
C_I	ADDR[30..14], RD_/WR, /WE_AT[1..0], /CS-ETK	30 pF
C_I	/OE	22 pF
C_I	/HRESET	10 pF
C_I	/PORESET	19 pF

note

*:/SGRES: opendrain FET; I_{Dmax} = 0.2 A
Capacitance only with ETK-logic, without MPC, PCB and BGA socket

4.3.3 Switching Characteristics

The following diagrams show the timings the ETKP5.0 can process.

Para.	Description	Min	Max	Unit
t_4	Access Cycle Time	20		ns
t_6	Chip Select Valid to Data Valid		20	ns
t_9	Address Valid to Data Valid		20	ns
t_{10}	Read Low to Data Valid		12	ns
t_{11}	Read Low Z-Time	3		ns
t_{12}	Read High Z-Time		12	ns
t_{16}	Chip Select Setup Time	0		ns
t_{17}	Chip Select Hold Time	0		ns
t_{21}	Address Valid to End of Write	16		ns
t_{22}	Data Setup Time	12		ns
t_{23}	Data Hold Time	0		ns
t_{24}	Read/Write Setup Time	0		ns
t_{25}	Read/Write Hold Time	0		ns
t_{31}	Byte Enables Setup Time	0		ns
t_{32}	Byte Enables Width	17		ns
t_{33}	Byte Enables Hold Time	0		ns
t_{46}	Chip Select Invalid to High Z-Time		12	ns
t_{47}	Byte Enables Valid to Data Valid		20	ns
t_{48}	Byte Enables Invalid to High Z-Time		12	ns

note

All timings are measured at a reference level of 1.5 V. Output signals are measured with 10 pF to ground and 50 Ω to 1.5 V.

Fig. 4-1   Read Cyle: Data Emulation and Measurement Data DPR

*Write Timing: Data Emulation and Measurement Data DPR*

.
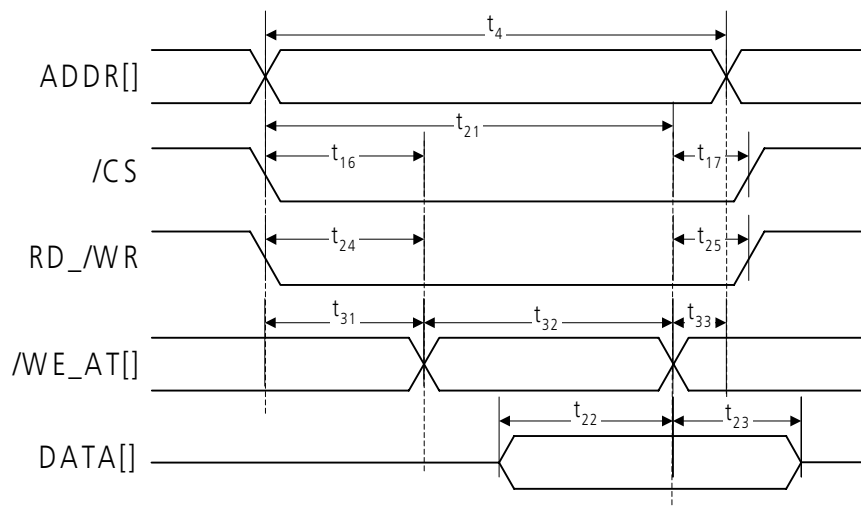
Fig. 4-2   Write Cycle: Data Emulation and Measurement Data DPR

4.4 Mechanical Dimensions

The reference measure for all drawings is millimeter.

4.4.1 ETKP5.0 Dimensions

Dimensions	Millimeters	Inches
Length	64.00	2.520
Width	61.00	2.403
Thickness of PCB	1.70	0.067
Height of component (upper side)	3.00	0.118
Height of component (lower side)	2.00	0.079
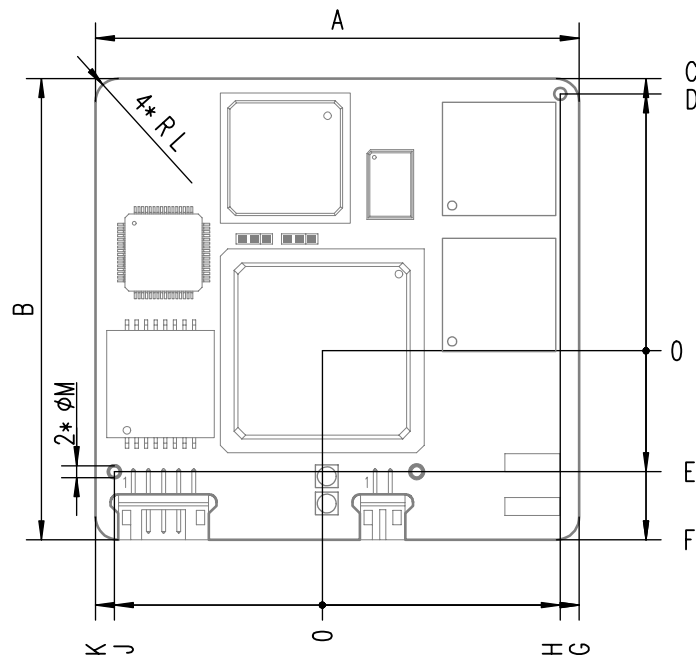
Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	64.00	2.520	**G**	34.00	1.339
B	61.00	2.403	**H**	31.50	1.241
C	36.00	1.418	**J**	27.50	1.083
D	34.00	1.339	**K**	30.00	1.182
E	16.00	0.630	**L**	3.00	0.118
F	25.00	0.985	**M**	1.50	0.059
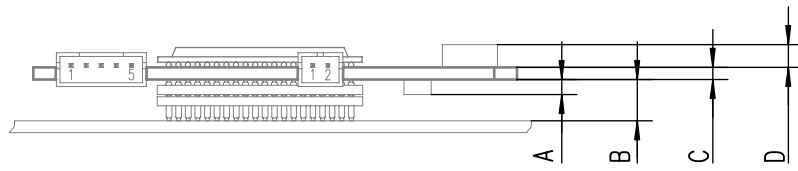
Fig. 4-3 Mechanical Dimensions: Micro directly soldered

Dim	Millimeters	Inches
A	2.00	0.079
B	5.77	0.227
C	1.70	0.067
D	3.00	0.118

4.5   Interface Cables

Interface Cable KA41 for Insert Socket, Proposal 1
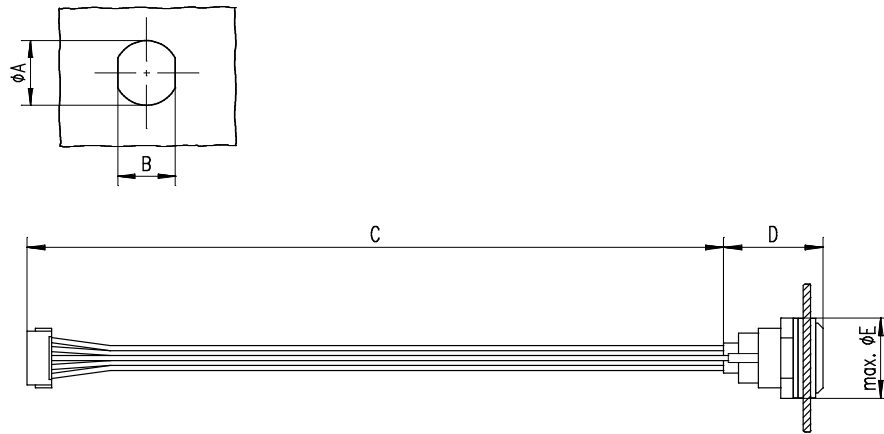
Fig. 4-4   Interface Cable KA41, Prop. 1

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	13.90	0.547	D	20.00	0.787
B	12.30	0.484	E	16.20	0.636
C	140.00	5.512			

note

Shield not connected to ECU housing.
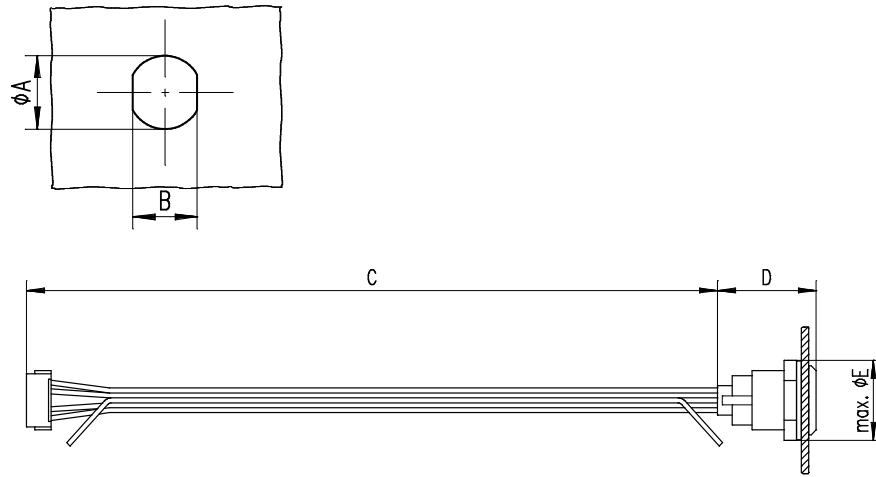
Fig. 4-5   Interface Cable KA41, Prop. 2

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	12.10	0.476	**D**	20.00	0.787
B	10.60	0.417	**E**	16.20	0.636
C	140.00	5.512			

note

Shield connected to ECU housing. Insulating disc must be removed.

Fig. 4-6   Interface Cable KA54, Prop. 1

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	12.50	0.492	**C**	400.00	15.748
B	160.00	6.299	**D**	19.00	0.748

note

Shield connected to ECU housing.

SKINDICHT *compact screwing;* **Manufacturer**: *Lapp;* **Description**: *SH7;* **Order-No.**: *5200 0830*

Nut for compact screwing; **Manufacturer:** *Lapp;* **Description:** *SM7;* **Order-No.:** *5200 3490*

Interface Cable KA54 with PG-screwing, Proposal 2
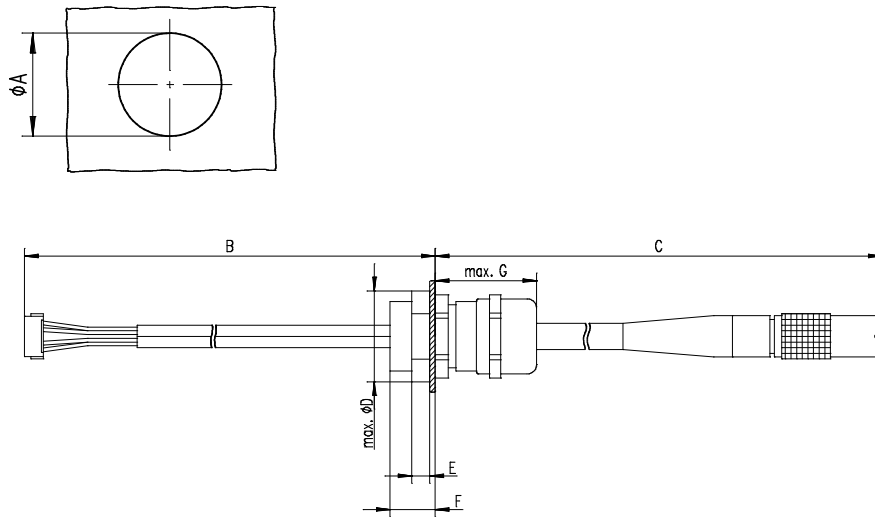
Fig. 4-7   Interface Cable KA54, Prop. 2 (long thread)
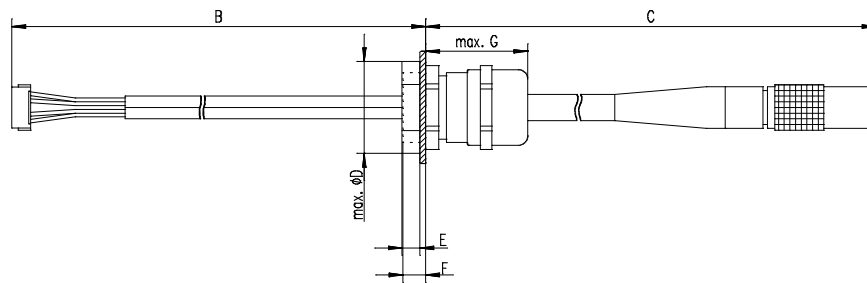
Fig. 4-8   Interface Cable KA54, Prop. 2 (short thread)

Dim	Millimeters	Inches	Dim	Millimeters	Inches
A	18.80	0.740	**E**	4.70	0.185
B	160.00	6.299	**F**$_{Long}$	12.00	0.472
C	400.00	15.748	**F**$_{Short}$	6.00	0.263
D	24.25	0.955	**G**	27.00	1.063

note

Shield connected to ECU housing.

SKINTOP *compact screwing;* **Manufacturer:** *Lapp;* **Description:** *MS-SC 11 ;* **Order-No.:** *5311 2320 (long thread) or 5311 2220 (short thread)*

Nut for compact screwing; **Manufacturer:** *Lapp;* **Description:** *SM-PE 11 ;* **Order-No.:** *5210 3220*

Interface Cable KA55
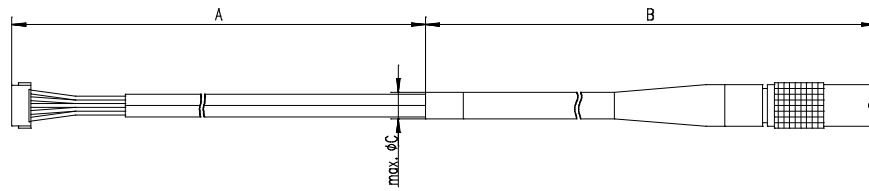
Fig. 4-9   Interface Cable KA55

Dim	Millimeters	Inches
A	160.00	6.299
B	400.00	15.748
C	7.50	0.295

note

Strain relief on ECU cover necessary. Shield not connected to ECU housing.

Fig. 4-10   Interface Cable KA56

Dim	Millimeters	Inches
A	670.00	26.378
B	70.00	2.756
C	340.00	13.386
D	260.00	10.236
E	95.00	3.740
F	165.00	6.496

note

Shield connected to ECU housing.

4.6   Power Supply Cables

Cable ETV
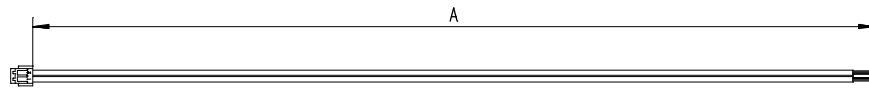
Fig. 4-11   Power Supply Cable ETV

Dim	Millimeters	Inches
A	190.00	7.480

Cable with Filtercoil ETV2
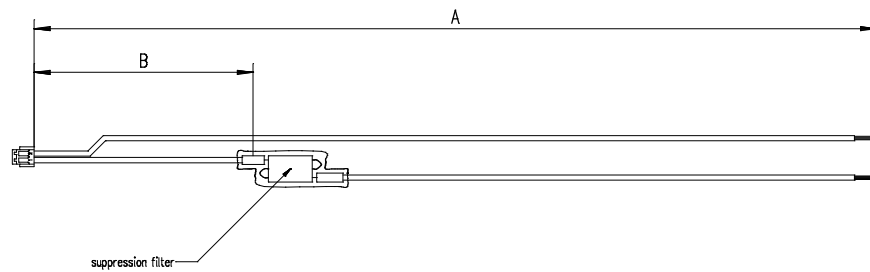
Fig. 4-12   Power Supply Cable with Filtercoil ETV2

Dim	Millimeters	Inches
A	190.00	7.480
B	50.00	1.969

Cable with Filtercoil KA57
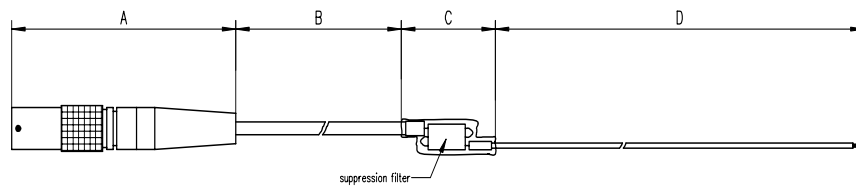
Fig. 4-13   Power Supply Cable with Filtercoil KA57

Dim	Millimeters	Inches	Dim	Milimeters	Inches
A	60.00	2.362	C	40.00	1.575
B	400.00	15.748	D	165.00	6.496

note

Ground must be supplied separately.

5   Ordering Information

Type	Order-No.	Note
ETKP5.0	customer-specific	MPC555 to be supplied by customer
Interface Cables:		
KA41, Prop. 1 / Prop. 2	Y 261 A24 729	
KA54, Prop. 1 / Prop. 2	F 00K 001 302	Delivery without PG-screwing
KA55	F 00K 001 303	
KA56	F 00K 001 654	
Power Supply Cables:		
ETV	Y 261 A24 446	
ETV2	F 00K 000 593	
KA57	F 00K 001 655	

6   Revision History

Revision	Date	Changes
1.0.1	2001/08/28	Initial Version
1.0.2	2002/02/04	Updated chip select section

List of Figures

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