Product :	ETKP7.0
Title :	Change Information
File :	ETKP70_Change_Information_V1.3.doc
TTN :	F-00K-103-199 – ETKP7.0-K F-00K-103-197 – ETKP7.0-A
Comments :	Currently shipped: 24E013 FPGA-Code version: V2.4 Hardware-state: E013

	Name	Department	Signature	Date / Release Date
Created:	Mai	ETAS / PHW-EES1	Mai	24.04.2008
Released:	Meerwein	ETAS / PHW-EES21	Meerwein	24.04.2008

Changes

Revision	Description	Date	Name	Signature
1.0	20B013 - initial version of the new product	27.11.2002	Müller	Müller
1.1	New product variant ETKP7.0-A released	13.08.2004	Müller	Müller
1.2	23E013 - HW redesign due to discontinuation of some components	08.05.2007	Mai	Mai
1.3	24E013 – new FPGA version – measurement problem due to wrong trigger segment address decoding	24.04.2008	Mai	Mai

Table of Contents

1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.
Two different items are described.

- Explanation of the version-system of the ETKP7.0
- The required versions of software (INCA / ASCET) , HSP (calibration hardware firmware of e.g. ES690, ES1232, MAC2...) and ETK - hardware.
  Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

2 Tool-Chain Information

2.1 Version-Syntax of the ETKP7.0

The ETKP7.0 version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: aacddd/ee

PLD-Code Information:
- aa: FPGA-Code version (10, 11, 12,...) — see chapter 3

Hardware-Information:
- c : PCB version (A, B, C, ...)
- ddd: Hardware state of the PCB (010, 011, 012, ...) — see chapter 4
- ee: Assembly variant of the PCB (00, 01, 02, ...)

The first delivered hardware state of the ETKP7.0 was 20B013/01.

Customer variants of this ETK will be additionally differentiated using different letters in the name (ETKP7.0-A, ETKP7.0-B, ...) and different product item numbers.

2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.
If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
HSP - Customer Test Version	1.3.1	First delivered beta version: HSP-ETK-CTV - V201.3.1
HSP	2.0	First released HSP version, will be delivered separately from INCA
MAC2	✓	Supported
ES690	✓	Supported
ES1000.2-system	✓	ES1200/1, ES1231 and ES1232 supported with ES1120
ES1000.1	✕	ES1111 (VCU1) will not be supported
Software		
VS100	Not supported	
DOS ETK-Config-Tool	Not supported	
ETK Configuration Tool	V 1.5.2	
INCA - Customer Test Version	V 4.0.1	With the following beta packages: • EtkAccess-CTV-EtkP7 - V6.0.1 • HSP-ETK-CTV - V201.3.1
INCA	V 4.0.2	ETKP7.0-x (basic, compatibility and advanced mode)

The registered user will automatically receive the newest INCA-version (CD-ROM)
Updates or refreshes can be downloaded from the ETAS homepage:
http://de.etasgroup.com
http://en.etasgroup.com

3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETKP7.0 is stored onto programmable logic devices (FPGA). The FPGA-code starts with version 2.0. For the version syntax please refer to chapter 2.1.

3.2 FPGA-Code version 2.0 was the first delivered version

3.2.1 Details of change

Version 2.3:	update file dated 25.04.2007
Cause:	As some components of the ETKP4 HW Revision B are discontinued, a new FPGA code is needed
Hint:	This new HDC is only valid for the HW Revision E
Version 2.4:	update file dated 21.04.2008
Error:	Measurement with ETK will not work, when using trigger segment address ending with 0x40 or 0xC0
Remedy:	Trigger segment address decoding in FPGA changed
Hint:	This new HDC is only valid for the HW Revision E
Attention:	For updating the ETK - HDC with a later version by using the ETK - configuration tool, all ETK - FPGA - packages will be updated one after another and will last a few minutes.

3.2.2 Delivery condition

The FPGA version 2.4 will be programmed into all shipments.

4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts require a part assembly changing of this ETK. Information about changes are listed below within this chapter. The hardware-state is versioned beginning with version 013. For the versioning syntax please refer to chapter 2.1.

4.2 Changes from Hardware-state B013 to version E013

4.2.1 Details of change

Changes: HW had to be redesigned due to obsolete components.
The electrical characteristics remained the same!

4.2.2 Delivery condition

The hardware-state E013 will be delivered with all new shipments.
B-Revision ETKP7 can not be upgraded to the E-Revision!

4.3 Assembly-Variant

Assembly-Variant		
Rev.	Variant	Description
B	00	ETKP7.0-K (socket) with /CS2
	01	ETKP7.0-A (socket) with /CS0
E	01	ETKP7.0-K (socket) with /CS2
	02	ETKP7.0-A (socket) with /CS0

5 Abbreviations

ETK	Emulator test probe
INCA-VME	Old VME - system for MC and RP
ES1000.1	VME - system, successor of the INCA-VME contains the ES1111 (VCU1)
ES1000.2	VME - system, successor of the ES1000.1 contains the ES1120 (VCU2)
MAC2	Old MC hardware
ES690	MC hardware, successor of MAC2
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	Hardware Service Pack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	Measurement & Calibration
RP	Rapid Prototyping
PLD	Programmable Logic Device
FPGA	Free Programmable Gate Array; interface component to the application hardware
PCB	Printed Circuit Board
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select