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File :	ETKS1.1-C_Change_Information_V1.1.doc			
TTN :	F-00K-102-964			
Comments :	Currently shipped: (12)14A010 (FPGA-Boot-Code version: V1.2) FPGA-B version: V1.4 Hardware-state: A010			
Created:	Name Müller	Department PAC-P3	Signature Müller	Date 04.09.2003
Released:	Name Maier	Department PAC-P3	Signature Maier	Date 04.09.2003

Changes

Revision	Description	Date	Name	Signature
1.0	(10)10A010 - initial version	25.03.2002	Müller	Müller
1.1	(12)14A010 - coldstart functionality enabled [chapter 3.2.1 & 3.3.1]	01.09.2003	Müller	Müller

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1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.

Two different items are described.

- Explanation of the version-system of the ETKS1.1-C
- The required versions of software (INCA / ASCET) , HSP (calibration hardware firmware of e.g. ES690, ES1232, MAC2...) and ETK - hardware.

Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK

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2 Tool-Chain Information

2.1 Version-Syntax of the ETKS1.1-C

The ETKS1.1-C version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: **(aa₀)aa₁cddd/ee**

PLD-Code Information:

(aa₀): FPGA-Boot-Code version (10, 11, 12,...) see chapter 3

The FPGA-Boot-Code version is not printed onto the ETK - label.

aa₁: FPGA-C-Code version (10, 11, 12,...) see chapter 3

Hardware-Information:

c : PCB version (A, B, C, ...)

ddd: Hardware state of the PCB (010, 011, 012, ...) see chapter 4

ee: Assembly variant of the PCB (00, 01, 02, ...)

The first delivered hardware state of the ETKS1.1-C was **(10)10A010/01**.

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2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it.

If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
HSP	V 1.0	First HSP version will support ETKS1.1-C
MAC2	V 4.1.9	Supported
ES690	✓	Supported
ES1000.2-system	V 4.1.9	ES1200/1, ES1231 and ES1232 supported with ES1120
ES1000.1	V 4.1.9	Supported
Software		
VS100	Not supported	
DOS ETK-Config-Tool	Not supported	
ETK Configuration Tool	V 1.4.3	
INCA	V 3.1.3	(basic mode)

Support coldstart:

Name	Needed version	Remarks
MAC2	✗	Coldstart will not be supported by MAC2
ES1000.1	✗	Coldstart will not be supported by ES1111 (VCU1)
HSP	V 2.2	By using the new features without the mentioned HSP, problems will occur.
INCA	V 4.0.3	By using the new features without the mentioned INCA, problems will occur. (basic mode)

The registered user will automatically receive the newest INCA-version (CD-ROM)

Updates or refreshes can be downloaded from the ETAS homepage:

<http://de.etasgroup.com>

<http://en.etasgroup.com>

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3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETKS1.1-C is stored onto programmable logic devices (FPGA). The FPGA-code starts with version 1.0. For the version syntax please refer to chapter 2.1.

3.2 FPGA-Boot-Code version 1.0 was the first delivered version

3.2.1 Details of change

Version 1.2: file dated 12.11.2002
Cause: Manufacturing test enlarged in order to achieve a better product quality. A new FPGA-Boot code was necessary.

Attention: cçê=ì éÇ~íáãÖ=íÜÉ=bqh=J=ea`=í áíÜ=íÜÉ=ä~íÉëí=í Éëääçã=Äó=ì eääÖ=íÜÉ bqh=J=ÄçãÑáÖì ê~íáçã=íççãì=-ää=bqh=J=cmd^=J=e~Äâ~ÖÉë=í äää=ÄÉ=ì éÇ~íÉÇ çãÉ=ÑíÉê=ãçíÜÉêK

3.2.2 Delivery condition

The FPGA-Boot version **1.2** will be programmed into all shipments.

3.3 FPGA-C-Code version 1.0 was the first delivered version

3.3.1 Details of change

Version 1.4: file dated 20.11.2002
New feature: Coldstart enabled and ECU start-up communication improved.
Error 1: After an ECU reset the first access to the ETK could fail.
Remedy: New FPGA-C code provides the new functionality and bugfix. In order to get rid of Error 1, the ETK behaviour after ECU access timeout has been improved.

Attention: cçê=ì éÇ~íáãÖ=íÜÉ=bqh=J=ea`=í áíÜ=íÜÉ=ä~íÉëí=í Éëääçã=Äó=ì eääÖ=íÜÉ bqh=J=ÄçãÑáÖì ê~íáçã=íççãì=-ää=bqh=J=cmd^=J=e~Äâ~ÖÉë=í äää=ÄÉ=ì éÇ~íÉÇ çãÉ=ÑíÉê=ãçíÜÉêK

3.3.2 Delivery condition

The FPGA-C version **1.4** will be programmed into all new shipments.

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4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes are listed underneath. The hardware-state starts with version A010. For the version syntax please refer to chapter 2.1.

4.2 No changes at hardware-state A010

4.2.1 Delivery condition

The hardware-state **A010** will be delivered with all shipments.

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5 Abbreviations

ETK	Emulator test probe
ES1000	VME - system, successor of INCA-VME
INCA-VME	Old VME - system for MC and RP
ES690	MC hardware, successor of MAC2
MAC2	Old MC hardware
INCA	MC software, successor of VS100
VS100	MC software
ETK Configuration Tool	Configuration Software, in order to configure an ETK, successor of the old DOS tool
DOS ETK-Config-Tool	Old configuration software, in order to configure an ETK
HSP	H ardware S ervice P ack; ETAS product which includes the firmware for the complete ETAS hardware, shipped together with INCA but also available as standalone product, download at ETAS homepage possible
Firmware	Software for MC hardware; necessary for implementation of new features or bugfixes
Hotfix	Software bugfix for a refresh version
Tool-chain	MC hardware (e.g. ES690) and software (e.g. INCA)
MC	M easurement & C alibration
RP	R apid P rototyping
PLD	P rogrammable L ogic D evice
FPGA	F ree P rogrammable G ate A rray; interface component to the application hardware
PCB	P rinted C ircuit B oard
DPR	Dual Ported RAM; special RAM onto the ETK which allows an access from ECU and application hardware at the same time
/CS	Chip select