

ETAS Entwicklungs- und Applikationswerkzeuge für elektronische Systeme GmbH

Product:	ETK-S5.1	Rev:	04	Page 1 of 7
Title :	Release Notes/Change Information			

Product :	ETK-S5.1	ETK-S5.1			
Title :	Release Note	s / Change Informatio	n		
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TTN:	ETK-S5.1	ETK-S5.1 F-00K-103-866			
Comments :	FPGA version	Currently shipped: 24A011/02 FPGA version: V2.4 Hardware-state: A011			
Created:	Name Higgins	Department PHW/EPM31	Signature Higgins	Date Nov 5, 2007	
Released:	Name Collins	Department PHW/EPM32	Signature Collins	Date Nov 8, 2007	

Changes

Revision	Description	Date	Name	Signature
1.0	20A010/02 - initial Version	Apr 20, 2005	Collins	Collins
02	22A011/02 – QA3.1 Version with TDM & new uC support	May 23, 2006	Collins	Collins
03	23A011/02 – QA3.2 Version with Coldstart support & correct Reset Monitoring	July 16, 2007	Higgins	Higgins
04	24A011/02 – QA3.3 Version with additional ECU to ETK detection mechanism	Nov 5, 2007	Higgins	Higgins

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1 General remarks to this document

This document consists of three main parts.

Chapter 2 contains general information about the required tool-chain to use this ETK.

Two different items are described.

- Explanation of the version-system of the ETK-S5.1
- The required versions of software (INCA / ASCET), HSP (calibration hardware firmware of e.g. ES690, ES59x, ES1232, ..) and ETK - hardware.
 Additionally other requirements for running the ETK.

Chapter 3 contains information about PLD-Code changes concerning this ETK

Chapter 4 contains information about hardware changes concerning this ETK



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2 Tool-Chain Information

2.1 Version-Syntax of the ETK-S5.1

The ETK-S5.1 version information is located on the sticker of the ETK or can be read out of the ETK using the ETK-Configuration Tool.

The version information has the following syntax: aacddd/ee

PLD-Code Information:

aa: FPGA-Code version (10, 11, 12,...) see chapter 3

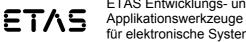
Hardware-Information:

c: PCB version (A, B, C, ...)

ddd: Hardware state of the PCB (010, 011, 012, ...) see chapter 4

ee: Assembly variant of the PCB (00, 01, 02, ...)

The first delivered hardware state of the ETK-S5.0 was 20A010/02.



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2.2 Version information of the Tool-Chain components

To get this ETK running with the other components of the ETAS Tool-Chain please make sure that the version mentioned below or a newer one is used. If your software-, firmware- or hardware version is older, please update it. If you have any problems to get this ETK running please contact our local customer support or sales representative.

Name	Needed version	Remarks
HSP	V 5.1.0	Note: HSP V6.1 required to configure new ECU to ETK detection mechanism introduced with HDC v2.3
ES690	V 10.0.2	
ES59x	V 10.0.2	
ES910.2	V 1.0	
ES1000.2/3	V 10.0.2	Supported with ES1232
MAC2, ES1000.1, ES1200/01, and ES1231		Not Supported
Software		
INCA	V 5.4.1	Note: INCA V6.1 required to configure new ECU to ETK detection mechanism introduced with HDC v2.3
ASCET-RP	V 5.4.0	
INTECRIO	V 1.1	

The registered user will automatically receive the newest INCA-version (CD-ROM) Updates or refreshes can be downloaded from the ETAS homepage:

http://de.etasgroup.com http://en.etasgroup.com



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3 PLD-Code Changes

3.1 General remarks to this chapter

The programmable logic code within the ETK-S5.0 is stored onto programmable logic devices (FPGA). The FPGA-code starts with version 2.0. For the version syntax please refer to chapter 2.1.

3.2 FPGA-Code version 2.0 is the first released version

3.2.1 Details of change

Version 2.0: Initial version

Version 2.2: Update file dated February 14, 2006

Cause: Request for new µC variant "GP5", enabling trigger direct

measurement, and removal of coldstart functionality

New FPGA file Remedy:

Attention: For updating the ETK - HDC with a later version by using the

ETK - configuration tool, all ETK - FPGA - packages will be updated

one after another and will last a few minutes.

Version 2.3: Update file dated July 16, 2006

Enabling coldstart functionality and re-definition of pin 15 to Cause:

monitor the uC reset status

Remedy: New FPGA file

Attention: For updating the ETK - HDC with a later version by using the

ETK - configuration tool, all ETK - FPGA - packages will be updated

one after another and will last a few minutes.

Version 2.4: Update file dated Oct 5, 2007

Cause: Additional ECU to ETK detection mechanism provided. To enable

the optional feature, minimum INCA / HSP versions are required; see

section 2.2 for details. For details about how to use the new

feature; refer to the latest ETK-S5.1 solution proposal.

Remedy: New FPGA file

Attention: For updating the ETK - HDC with a later version by using the

ETK - configuration tool, all ETK - FPGA - packages will be updated

one after another and will last a few minutes.

3.2.2 Delivery condition

The FPGA version **2.4** will be programmed into all shipments.



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4 Hardware Changes

4.1 General remarks to this chapter

Hardware problems or obsolete parts can make it necessary to change the manufacturing of this ETK. Information about the changes are listed below. The hardware-state starts with version A010. For the version syntax please refer to chapter 2.1.

4.2 Hardware-state A010 is the first delivered version

4.2.1 Details of Change

See Project 1608, ETKS1.1 for details on hardware state changes

4.2.2 Delivery condition

The hardware-state **A011** will be delivered with all new shipments.



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5 Abbreviations

Emulator test probe
VME - system, successor of INCA-VME
Old VME - system for MC and RP
MC hardware, successor of MAC2
Old MC hardware
MC software, successor of VS100
Configuration Software, in order to configure an ETK,
successor of the old DOS tool
Hardware Service Pack; ETAS product which includes
the firmware for the complete ETAS hardware,
shipped together with INCA but also available as
standalone product, download at ETAS homepage
possible
Software for MC hardware; necessary for
implementation of new features or bugfixes
Software bugfix for a refresh version
MC hardware (e.g. ES690) and software (e.g. INCA)
Measurement & Calibration
Rapid Prototyping
Programmable Logic Device
Field Programmable Gate Array; interface component
to the application hardware
Printed Circuit Board
Dual Ported RAM; special RAM onto the ETK which
allows an access from ECU and application hardware
at the same time
Chip select