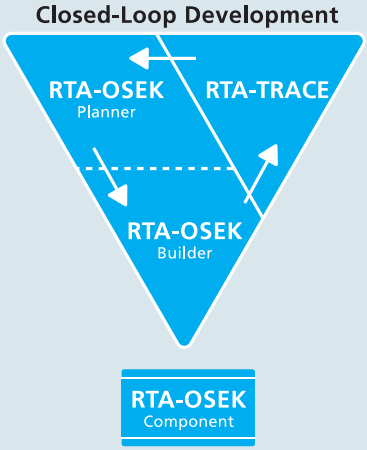
RTA-OSEK
Texas Instruments TMS570 with the TI Compiler



Features at a Glance

- OSEK/VDX OS v2.2 Certified OS
- RTOS overhead: 28 bytes RAM, 176 bytes ROM
- Category 2 interrupt latency: 214 CPU cycles
- Applications include: Chassis Control, Occupant Safety Systems, Gateways

ETAS Group
Automotive LifeCycle Solutions

RTA-OSEK

RTA-OSEK provides an application design environment that combines the smallest and fastest OSEK RTOS with an unique timing analysis tool.

This port data sheet discusses the Texas Instruments TMS570 port of the RTA-OSEK kernel alone and should be read in conjunction with the Technical Product Overview "*Developing Embedded Real-Time Applications with RTA-OSEK*" available from ETAS.

The kernel element of RTA-OSEK is a fixed priority, pre-emptive real-time operating system that is compliant to the OSEK/VDX OS standard version 2.2 for all four conformance classes (BCC1, BCC2, ECC1 and ECC2) and intra processor communication using OSEK COM Conformance Classes A and B (CCCA and CCCB).

All CPU overheads of the kernel have low worst case bounds and little variability in execution time. The kernel is particularly suited to systems with very tight constraints on hardware costs and where run-time performance must be guaranteed.

The kernel is configured using an offline tool provided with RTA-OSEK. Determining in advance which features are used allows memory requirements to be minimized and API calls to be optimized for greatest efficiency.

All tasks and ISRs in RTA-OSEK run on a single stack – even extended tasks. This allows dramatic reductions in application stack space requirements.

The RTA-OSEK kernel is designed to be scalable. When a task uses queued activation or waits on events, the additional RTOS overhead required to support these features is paid by the task rather than by the system. This means that a basic single activation task uses the same resources in a BCC1 system as it does in an ECC2 system.

Compiler/Assembler/Linker

The libraries containing the code for the RTA-OSEK kernel have been built using the following tools:

- Texas Instruments cl470.exe v4.4.0
- Texas Instruments cl470.exe.v4.4.0

- Texas Instruments lnk470.exe v4.4.0

Memory Model

RTA-OSEK supports a flat 32-bit memory model. The only restrictions placed on memory usage are that locations used by on-board peripherals cannot be used for application code and the vector table must be located at 0x0.

ORTI Debugger Support

ORTI is the OSEK Run-Time Interface that is supported by RTA-OSEK for the following debugger:

- Lauterbach Trace32

Further information about ORTI for RTA-OSEK can be found in the ORTI Guide.

Hardware Environment

RTA-OSEK supports all variants of the Texas Instruments TMS570 CPU family, including TMS470PSF761 and TMS470PVF81x.

Interrupt Model

RTA-OSEK for the TMS570 supports multiple interrupt priority levels. These correspond to values in the REQMASK register of the VIM module. The two highest priority VIM channels that are hard wired to the FIQ interrupt can only support Category 1 interrupts. All other VIM channels can be either Category 1 or 2. An interrupt can also be attached to the phantom interrupt (i.e. channel index 0). FIQ interrupts can be configured using the FIRQPR register. It is the user's responsibility to ensure this register is correctly configured for the priority scheme desired. Processor exceptions are only supported as Category 1 interrupts. When processing either Category 1 or 2 interrupts, no stack is used in IRQ mode. Instead, the processor mode is changed to Supervisor mode prior to any stack use.

Floating Point Support

RTA-OSEK for the TMS570 is designed to work with fully re-entrant software floating-point libraries supplied by Texas Instruments Inc. This allows floating-point to be used in RTA-OSEK tasks and ISRs without the need to save and restore any additional context.

Evaluation Board Support

RTA-OSEK can be used with any Texas Instruments Inc. TMS570 CPU evaluation board. An example application is provided to run on the Texas Instruments Inc. TMS470PSF761PZ Adapter Board evaluation board. This application can be adapted for other target boards by adjusting the linker command file (eg, to alter the allocation of program sections) and one source file (if alternative output pins are required).

Functionality

The table below outlines the restrictions on the maximum number of operating system objects allowed by RTA-OSEK.

	BCC1	BCC2	ECC1	ECC2
Max no of tasks	32 plus an idle task			
Max tasks per priority	1	32	1	32
Max queued activations	1	255	1	255
Max events per task	n/a	n/a	32	32
Max nested resources	255			
Max alarms	Not limited by RTA-OSEK			
Max standard resources	255			
Max internal resources	Not limited by RTA-OSEK			
Max application modes	65535			

Note that OSEK specifies that queued activations in an ECC2 system are only possible for basic tasks. Where tasks share a priority level, the maximum number of queued activations per priority level is 255.

The number of alarms, tasksets, schedules and schedule arrivalpoints is only limited by available hardware resources.

Memory Usage

The memory overhead of RTA-OSEK is:

Memory Type	Overhead (bytes)
RAM	28
ROM/Flash	176

In addition to the RTOS overhead, each object used by an application has the following memory requirements:

Object	RAM Bytes	ROM Bytes
BCC1 task	0	44
BCC2 task	10	60
ECC1 task	56	68
ECC2 task	58	76
Category 1 ISR	0	0
Category 2 ISR	0	120
Resource	0	20
Internal Resource	0	0

Object	RAM Bytes	ROM Bytes
Event	0	4
Alarm	12	36
Counter	4	40
Taskset (RW)	4	4
Taskset (RO)	0	4
Schedule	16	36
Arrivalpoint (RW)	12	12
Arrivalpoint (RO)	0	12

In addition to these static memory requirements each task priority and Category 2 interrupt has a stack overhead (in addition to application stack usage). The single stack model means that this overhead applies to each priority level rather than to each task. Similarly, for Category 2 interrupts this overhead applies for each unique interrupt priority. The table below shows stack usage for these objects.

Object	Stack Bytes
Task priority level	88
Category 2 interrupt	64

RTA-OSEK provides an optimization for task termination if the user can guarantee that tasks only terminate from their entry function. Tasks that terminate from elsewhere are not eligible for this optimization and duly require 56 more stack bytes per priority level than indicated in the table above.

Performance

The following table gives the key kernel timings for operating system behavior in CPU cycles.

Task Type	Basic	Extended	Ref
Category 1 ISR latency	90	90	K
Category 2 ISR entry latency	214	212	A
Category 2 ISR exit latency	386	564	E
Normal Termination	312	562	D
ChainTask	598	1220	J
Pre-emption	518	706	C
Triggered by alarm	884	1074	F
Schedule	486	664	Q
ReleaseResource	542	720	M
SetEvent	n/a	1110	S

All performance figures are for the non-optimized interface to RTA-OSEK. Using the optimized interface will result in shorter execution times for some operations. All tasks use lightweight termination and no pre or post task hooks were specified.

The execution time for every kernel API call is available on request from ETAS.

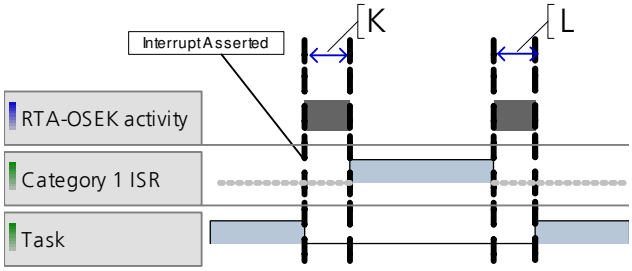


Figure 1 - Category 1 interrupt with return to interrupted task

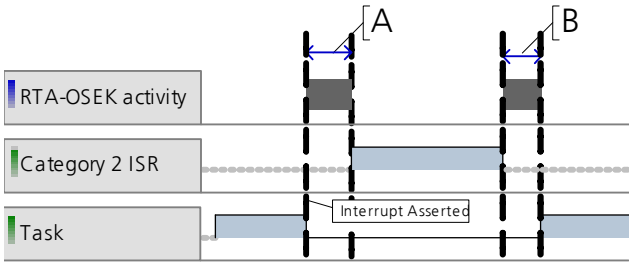


Figure 2 - Category 2 interrupt with return to interrupted task

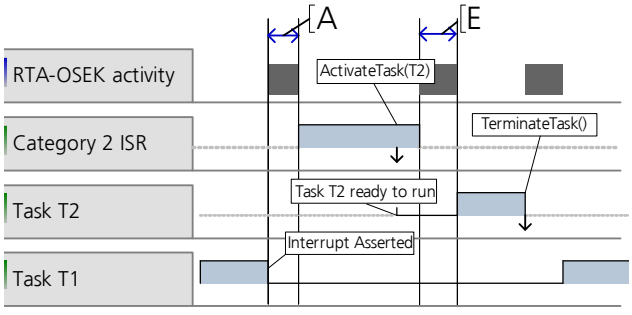


Figure 3 - Category 2 interrupt activates a higher priority task

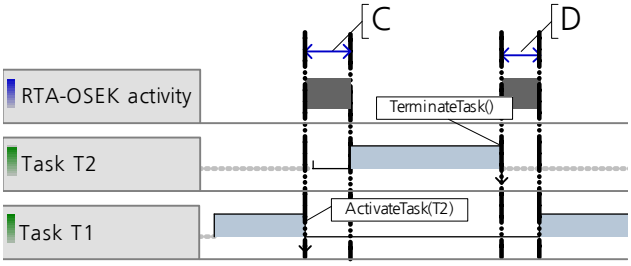


Figure 4 - Task activates a higher priority task

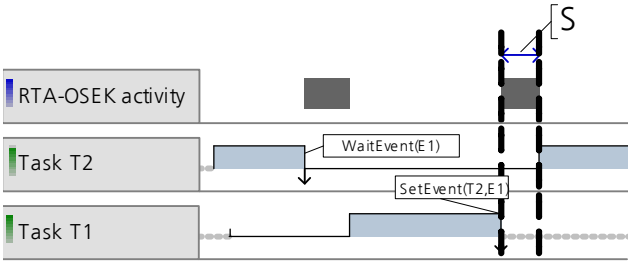


Figure 8 - Activation by SetEvent(

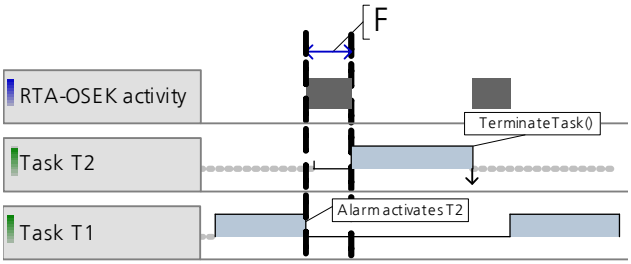


Figure 5 - Alarm activates task

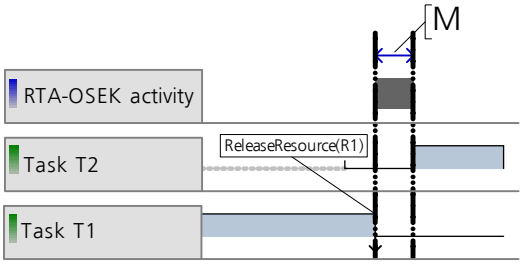


Figure 9 - ReleaseResource()

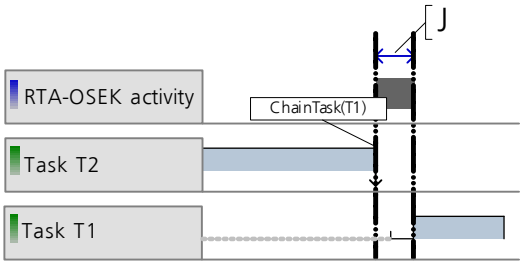


Figure 6 - Task chaining

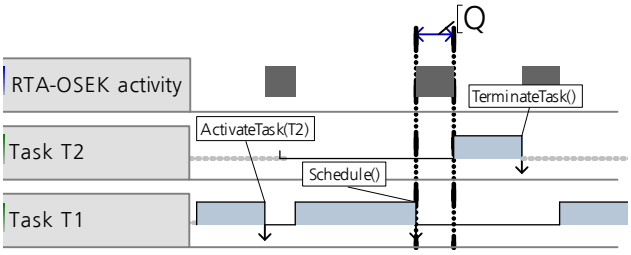


Figure 7 - Schedule() call

Benchmarks

The following sections shows benchmarks for RTA-OSEK memory usage for BCC1, BCC2, ECC1 and ECC2 conformant applications. The applications have the following framework:

- 8 tasks plus the idle task
- All basic tasks are lightweight tasks
- 1 Category 2 ISR with a 10ms minimum inter-arrival time
- 1 Counter
- 7 or 8 alarms, all attached to the same counter
- No resources or internal resources
- No hooks
- No schedules
- No tasksets
- Built using standard status

The following table shows the task priority configura-

tion for each benchmark application:

Task/ISR	Stack (bytes)	Period (ms)	BCC1	BCC2	ECC1	ECC2
ISR1	10	10	IPL1	IPL1	IPL1	IPL1
A	10	10	8	8	8	8
B	20	20	7	7	7	7
C	30	20	6	6	6	6
D	40	30	5	5	5	5
E	50	50	4	4	4	4
F	60	80	3	3	3	3
G	70	100	2	2	2	2
H	80	150	1	1	1	2
Idle	10	-	idle	idle	idle	idle

The overhead figures give the ROM and RAM required for RTA-OSEK in addition to that required by the application. The RAM figure is shown split into RAM data and RAM stack.

BCC1

The BCC1 application uses 8 basic tasks with unique priorities. This application has the following overheads:

Memory Usage	Bytes
OS ROM	**1928**
OS RAM	**920**
comprising RAM data	128
comprising RAM stack	792

BCC2

The BCC2 application uses 8 basic tasks with unique priorities.

Tasks A-G are attached to 7 alarms. Task H is activated multiple times from Task A and has maximum queued activation count of 255.

This application has the following overheads:

Memory Usage	Bytes
OS ROM	**2134**
OS RAM	**924**
comprising RAM data	124
comprising RAM stack	800

ECC1

The ECC1 application uses 7 basic tasks and 1 extended task with unique priorities. Task H is the extended task and it waits on a single event that is set by basic tasks A-G.

This application has the following overheads:

Memory Usage	Bytes
OS ROM	**2552**
OS RAM	**1072**
comprising RAM data	184
comprising RAM stack	888

ECC2

The ECC2 application uses 6 basic tasks and 2 extended tasks. Tasks G and H are the extended tasks and share a priority. The extended tasks wait on a single event that is set by tasks A-F.

This application has the following overheads:

Memory Usage	Bytes
OS ROM	**2950**
OS RAM	**1298**
comprising RAM data	250
comprising RAM stack	1048

Stack Optimization

Using stack optimization with the benchmark example identifies that the following tasks can share internal resources:

- "Tasks A, B and C
- "Tasks D, E and F
- "Tasks G and H

The benefit of this optimization is shown in the following table:

Total Stack Space (bytes)	BCC1	BCC2	ECC1	ECC2
Non-optimized	**1172**	**1180**	**1268**	**1428**
OS Overhead	792	800	888	1048
Application Overhead	380	380	380	380
Optimized	**532**	**532**	**628**	**628**
OS Overhead	352	352	448	448
Application Overhead	180	180	180	180

Notes

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ETAS/MKT61_Fi/07.2007