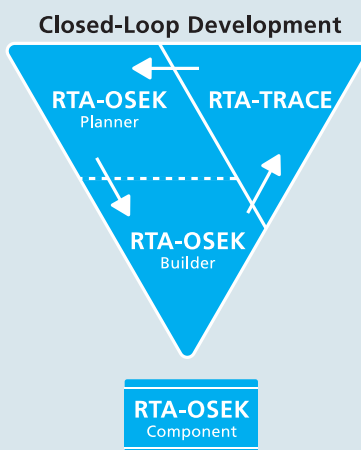


# RTA-OSEK

## Freescale MPC55xx/56xx with the WindRiver Compiler



### Features at a Glance

- OSEK/VDX OS v2.2 Certified OS
- RTOS overhead: 42 bytes RAM, 190 bytes ROM
- Category 2 interrupt latency: 133 CPU cycles
- Applications include: Engine Management, Integrated Starter Alternators, Chassis Control



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### RTA-OSEK

RTA-OSEK provides an application design environment that combines the smallest and fastest OSEK RTOS with a unique timing analysis tool.

This port data sheet discusses the Freescale MPC55xx and WindRiver compiler port of the RTA-OSEK kernel alone and should be read in conjunction with the Technical Product Overview "Developing Embedded Real-Time Applications with RTA-OSEK" available from ETAS.

The kernel element of RTA-OSEK is a fixed priority, pre-emptive real-time operating system that is compliant to the OSEK/VDX OS standard version 2.2 for all four conformance classes (BCC1, BCC2, ECC1 and ECC2) and intra processor communication using OSEK COM Conformance Classes A and B (CCCA and CCCB).

All CPU overheads of the kernel have low worst case bounds and little variability in execution time. The kernel is particularly suited to systems with very tight constraints on hardware costs and where run-time performance must be guaranteed.

The kernel is configured using an offline tool provided with RTA-OSEK. Determining in advance which features are used allows memory requirements to be minimized and API calls to be optimized for greatest efficiency.

All tasks and ISRs in RTA-OSEK run on a single stack – even extended tasks. This allows dramatic reductions in application stack space requirements.

The RTA-OSEK kernel is designed to be scalable. When a task uses queued activation or waits on events, the additional RTOS overhead required to support these features is paid by the task rather than by the system. This means that a basic single activation task uses the same resources in a BCC1 system as it does in an ECC2 system.

### Compiler/Assembler/Linker

The libraries containing the code for the RTA-OSEK kernel have been built using the following tools:

- Wind River Systems, Inc. DCC v5.8.0.0-2
- Wind River Systems, Inc. DAS v5.8.0.0-2

- Wind River Systems, Inc. DLD v5.8.0.0-2

### Memory Model

RTA-OSEK for the MPC55XX/Diab has a flat 32-bit memory model. For improved performance RTA-OSEK uses a small amount of RAM data that should be located in the compiler's Small Data Area. For all other objects 32-bit addressing is used externally providing no further restrictions on placement of user code and data.

### ORTI Debugger Support

ORTI is the OSEK Run-Time Interface that is supported by RTA-OSEK for the following debuggers:

- Lauterbach Trace32

Further information about ORTI for RTA-OSEK can be found in the *RTA-OSEK ORTI Guide*.

### Hardware Environment

RTA-OSEK supports all variants of the Freescale MPC55xx family i.e. MPC5533, MPC5534, MPC5553, MPC5554, MPC5561, MPC5565, MPC5566, MPC5567, MPC5514, MPC5516, MPC5674F, MPC5643L and MPC5644A.

### Interrupt Model

The RTA-OSEK MPC55xx/Wind River port supports 17 levels of interrupts. Category 1 and 2 interrupts handled by the peripheral interrupt controller (INTC) can be configured with priorities in the range of 1 to 15. CPU interrupts must be configured as Category 1 with a priority of 16. RTA-OSEK supports use of the INTC in either hardware or software vector modes. RTA-OSEK may also provide initialisation values for the Priority Select Registers.

### Floating Point Support

The Freescale MPC55xx can perform floating-point data manipulation in either software or hardware. Software floating-point handling in RTA-OSEK is designed to work with fully re-entrant software floating-point libraries supplied by Wind River Systems, Inc. Floating-point data can then be used in RTA-OSEK tasks and ISRs without the need to save and restore any additional context. To support hardware floating-point, "wrappers" are supplied to save and restore the additional context. To enable this functionality in this case, configure the relevant tasks and Category 2 ISRs as floating-point using the RTA-OSEK Planner and Builder tools.

### Evaluation Board Support

This port of RTA-OSEK can be used with any Freescale MPC55xx evaluation board. An example application is provided to run on the Axiom AXM-0123 with the

MPC5554 evaluation board. This application can be adapted for other target boards by adjusting the linker command file (e.g., to alter the allocation of program sections) and one source file (if alternative output pins are required).

### Functionality

The table below outlines the restrictions on the maximum number of operating system objects allowed by RTA-OSEK.

	BCC1	BCC2	ECC1	ECC2
Max no of tasks	64 plus an idle task			
Max tasks per priority	1	64	1	64
Max queued activations	1	255	1	255
Max events per task	n/a	n/a	32	32
Max nested resources	255			
Max alarms	Not limited by RTA-OSEK			
Max standard resources	255			
Max internal resources	Not limited by RTA-OSEK			
Max application modes	4294967295			

Note that OSEK specifies that queued activations in an ECC2 system are only possible for basic tasks. Where tasks share a priority level, the maximum number of queued activations per priority level is 255.

The number of alarms, tasksets, schedules and schedule arrivalpoints is only limited by available hardware resources.

### Memory Usage

The memory overhead of RTA-OSEK is:

Memory Type	Overhead (bytes)
RAM	42
ROM/Flash	190

In addition to the RTOS overhead, each object used by an application has the following memory requirements:

Object	RAM Bytes	ROM Bytes
BCC1 task	0	44
BCC2 task	10	64
ECC1 task	116	68
ECC2 task	118	76
Category 1 ISR	0	0
Category 2 ISR	0	64
Resource	0	24

Object	RAM Bytes	ROM Bytes
Internal Resource	0	0
Event	0	4
Alarm	12	48
Counter	4	128
Schedule Table	16	132
Schedule Table Expiry	0	12
Taskset (RW)	8	8
Taskset (RO)	0	8
Schedule	16	36
Arrivalpoint (RW)	16	16
Arrivalpoint (RO)	0	16

In addition to these static memory requirements each task priority and Category 2 interrupt has a stack overhead (in addition to application stack usage). The single stack model means that this overhead applies to each priority level rather than to each task. Similarly, for Category 2 interrupts this overhead applies for each unique interrupt priority. The table below shows stack usage for these objects.

Object	Stack Bytes
Task priority level	176
Category 2 interrupt	96

RTA-OSEK provides an optimization for task termination if the user can guarantee that tasks only terminate from their entry function. Tasks that terminate from elsewhere are not eligible for this optimization and duly require 112 more stack bytes per priority level than indicated in the table above.

## Performance

The following table gives the key kernel timings for operating system behavior in CPU cycles.

Task Type	Basic	Extended	Ref
Category 1 ISR Latency	82	82	K
Category 2 ISR Entry Latency	133	133	A
Category 2 ISR Exit Latency	230	426	E
Normal Termination	143	326	D
ChainTask	294	710	J
Pre-emption	234	420	C
Triggered by alarm	384	576	F
Schedule	217	404	Q
ReleaseResource	215	412	M

Task Type	Basic	Extended	Ref
SetEvent	n/a	791	S

All performance figures are for the non-optimized interface to RTA-OSEK. Using the optimized interface will result in shorter execution times for some operations. All tasks use lightweight termination and no pre or post task hooks were specified.

The execution time for every kernel API call is available on request from ETAS.

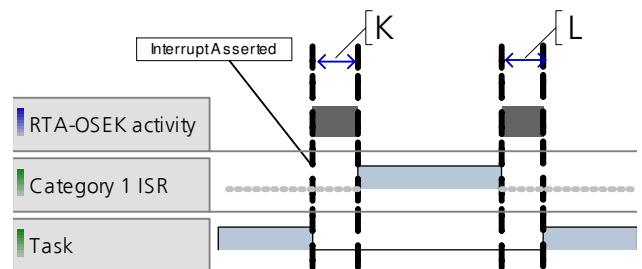


Figure 1 - Category 1 interrupt with return to interrupted task

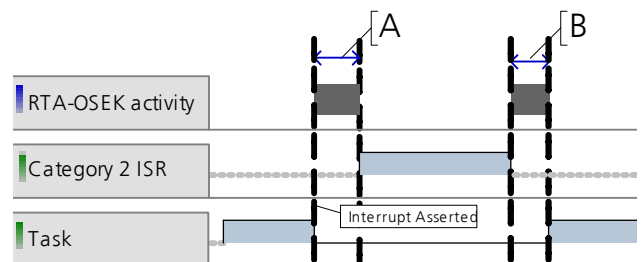


Figure 2 - Category 2 interrupt with return to interrupted task

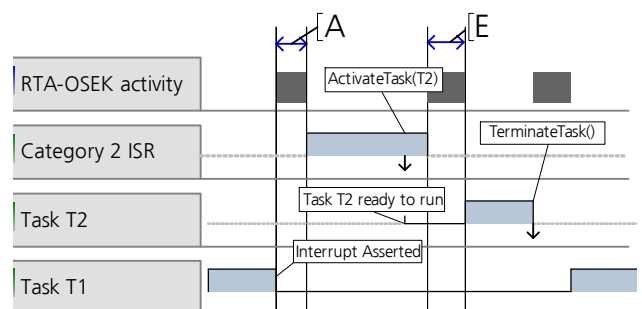


Figure 3 - Category 2 interrupt activates a higher priority task

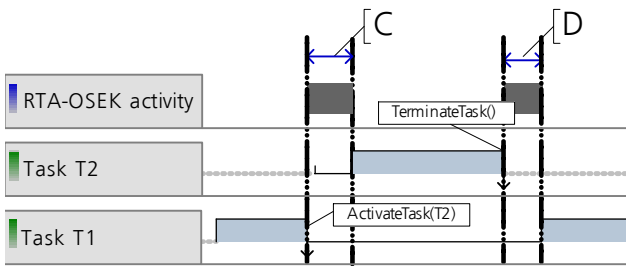


Figure 4 - Task activates a higher priority task

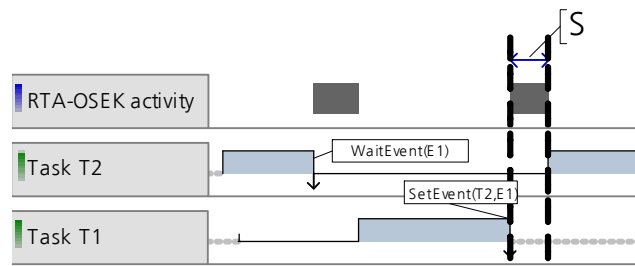


Figure 8 - Activation by SetEvent()

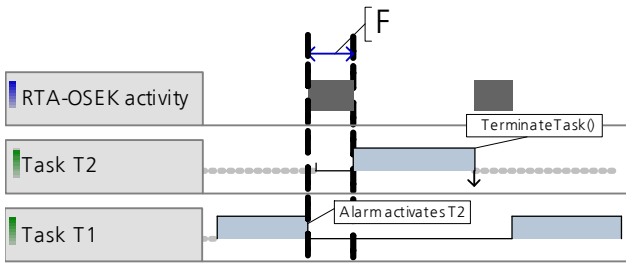


Figure 5 - Alarm activates task

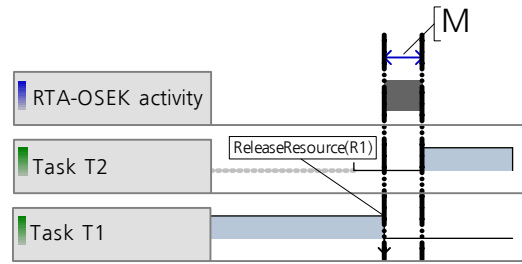


Figure 9 - ReleaseResource()

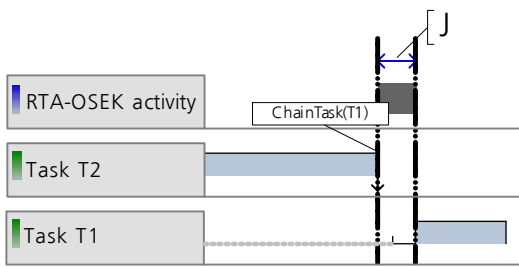


Figure 6 - Task chaining

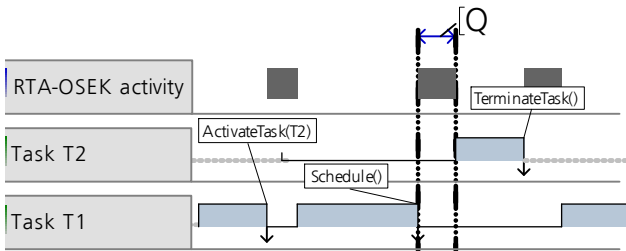


Figure 7 - Schedule() call

### Benchmarks

The following sections shows benchmarks for RTA-OSEK memory usage for BCC1, BCC2, ECC1 and ECC2 conformant applications. The applications have the following framework:

- 8 tasks plus the idle task
- All basic tasks are lightweight tasks
- 1 Category 2 ISR with a 10ms minimum inter-arrival time
- 1 Counter
- 7 or 8 alarms, all attached to the same counter
- No resources or internal resources
- No hooks
- No schedules
- No tasksets
- Built using standard status

The following table shows the task priority configura-

tion for each benchmark application:

Task/ISR	Stack (bytes)	Period (ms)	BCC1	BCC2	ECC1	ECC2
ISR1	10	10	IPL1	IPL1	IPL1	IPL1
A	10	10	8	8	8	8
B	20	20	7	7	7	7
C	30	20	6	6	6	6
D	40	30	5	5	5	5
E	50	50	4	4	4	4
F	60	80	3	3	3	3
G	70	100	2	2	2	2
H	80	150	1	1	1	2
Idle	10	-	idle	idle	idle	idle

The overhead figures give the ROM and RAM required for RTA-OSEK in addition to that required by the application. The RAM figure is shown split into RAM data and RAM stack.

### BCC1

The BCC1 application uses 8 basic tasks with unique priorities. This application has the following overheads:

Memory Usage	Bytes
<b>OS ROM</b>	<b>3326</b>
<b>OS RAM</b>	<b>1722</b>
comprising RAM data	158
comprising RAM stack	1564

### BCC2

The BCC2 application uses 8 basic tasks with unique priorities.

Tasks A-G are attached to 7 alarms. Task H is activated multiple times from Task A and has maximum queued activation count of 255. This application has the following overheads:

Memory Usage	Bytes
<b>OS ROM</b>	<b>3890</b>
<b>OS RAM</b>	<b>1734</b>
comprising RAM data	154
comprising RAM stack	1580

### ECC1

The ECC1 application uses 7 basic tasks and 1 extended task with unique priorities. Task H is the extended task and it waits on a single event that is set by basic tasks A-G. This application has the following overheads:

Memory Usage	Bytes
<b>OS ROM</b>	<b>4578</b>
<b>OS RAM</b>	<b>2014</b>
comprising RAM data	274
comprising RAM stack	1740

### ECC2

The ECC2 application uses 6 basic tasks and 2 extended tasks. Tasks G and H are the extended tasks and share a priority. The extended tasks wait on a single event that is set by tasks A-F. This application has the following overheads:

Memory Usage	Bytes
<b>OS ROM</b>	<b>5454</b>
<b>OS RAM</b>	<b>2444</b>
comprising RAM data	400
comprising RAM stack	2044

### Stack Optimization

Using stack optimization with the benchmark example identifies that the following tasks can share internal resources:

- "Tasks A, B and C
- "Tasks D, E and F
- "Tasks G and H

The benefit of this optimization is shown in the following table:

Total Stack Space (bytes)	BCC1	BCC2	ECC1	ECC2
<b>Non-optimized</b>	<b>1944</b>	<b>1960</b>	<b>2120</b>	<b>2424</b>
OS Overhead	1564	1580	1740	2044
Application Overhead	380	380	380	380
<b>Optimized</b>	<b>864</b>	<b>864</b>	<b>1040</b>	<b>1040</b>
OS Overhead	684	684	860	860
Application Overhead	180	180	180	180

## Notes

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Subject to change (11/2010)