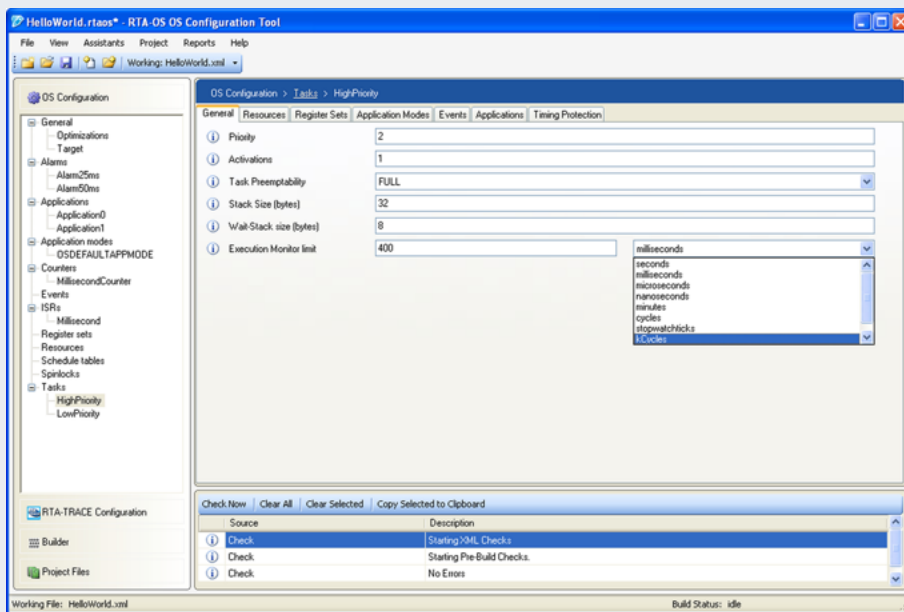


RTA-OS INFORMATION

Xilinx Zynq-7000 with the ARM Compiler



RTA-OS

RTA-OS is the new generation operating system from ETAS that conforms to the AUTOSAR OS specification and builds on the benefits of the successful RTA-OSEK product. It provides a toolsuite that includes a PC-based graphical configuration tool and adaptive OS generation capabilities to deliver flexible, fast solutions for a wide range of automotive microcontrollers.

The graphical configuration tool allows all OS objects to be configured, and creates AUTOSAR conformant XML files describing the OS configuration. In addition, it provides automatic verification against the AUTOSAR XML schema and allows users to create projects for easy management of multiple files.

RTA-OS improves on RTA-OSEK in several areas, including better runtime performance and smaller memory footprint,

support for multiple processor environments, and automatic support for up to 1024 tasks. The powerful performance analysis tools developed for RTA-OSEK have been updated for RTA-OS to allow hard real-time requirements to be met.

RTA Product Family

RTA-OS integrates seamlessly with other tools in the RTA product family, including:

- RTA-RTE – a mature, robust production quality AUTOSAR RTE Generator.
- RTA-TRACE – a software logic analyser that allows the runtime behaviour of RTA-OS to be observed.

Microcontroller Support

RTA-OS supports all variants of the Xilinx Zynq-7000 family of microcontrollers. Release testing has taken place using the Zynq-7020 variant.

Features at a Glance

AUTOSAR R4.0 compliant OS

Supports all scalability classes

MISRA-C:2004 compliant

RTOS overhead:
69 bytes RAM
0 bytes ROM

Category 2 ISR latency:
182 CPU cycles

Compiler Toolchain

RTA-OS for the Xilinx Zynq-7000 has been developed with the ARM v5.04 compiler.

Due to the adaptive code generation of RTA-OS, it is possible to use other versions of this compiler to build applications.

ORTI Debugger Support

RTA-OS can generate OSEK Runtime Interface information for the Lauterbach TRACE-32 debugger.

Interrupt Model

RTA-OS supports a nested interrupt model on the Xilinx Zynq-7000.

Memory Model

RTA-OS supports the standard 32 EABI memory model provided by the ARM compiler.

Maximum Number of OS Objects Allowed by RTA-OS

	BCC1	BCC2	ECC1	ECC2
Max. no. of tasks		Up to 1024		
Max. tasks per priority		Up to 1024		
Max. queued activations	1	$2^{32}-1$	1	$2^{32}-1$
Max. events per task	n/a	n/a	32	32
Max. alarms		$2^{32}-1$		
Max. software counters		$2^{32}-1$		
Max. hardware counters		$2^{32}-1$		
Max. nested resources		$2^{32}-1$		
Max. standard resources		$2^{32}-1$		
Max. internal resources		Not limited by RTA-OS		
Max. application modes		$2^{32}-1$		
Max. schedule tables		$2^{32}-1$		
Max. expiry points per schedule table		$2^{32}-1$		

Memory Overhead of RTA-OS

Memory Type	Overhead (bytes)
RAM	69
ROM/Flash	0

In addition to the OS overhead, each object used by a single-core application has the following memory requirements:

Object	RAM (bytes)	ROM (bytes)
Task	0	20
Category 2 ISR	0	8
Resource	4	8
Alarm	12	2
Counter	4	20
Schedule Table	12	16
Expiry Point	0	4

Performance

The following table gives the key RTA-OS kernel performance data measured in CPU cycles. All measurements were taken on a Xilinx Zynq-7020 with a 800MHz clock speed.

Task Type	Execution Time	Ref.
Pre-emption	128	A
Normal Termination	58	B
Task Switch	86	C
ChainTask	162	D
WaitEvent	264	E
SetEvent	336	F
Schedule	120	G
ReleaseResource	112	H
Category 2 ISR Entry Latency	182	I
Category 2 ISR Exit Latency resuming interrupted task	148	J
Category 2 ISR Exit Latency with task switch	140	K
Category 1 ISR Latency	160	L

The following figures illustrate how the RTA-OS kernel overheads are allocated during the operations given in the above table:

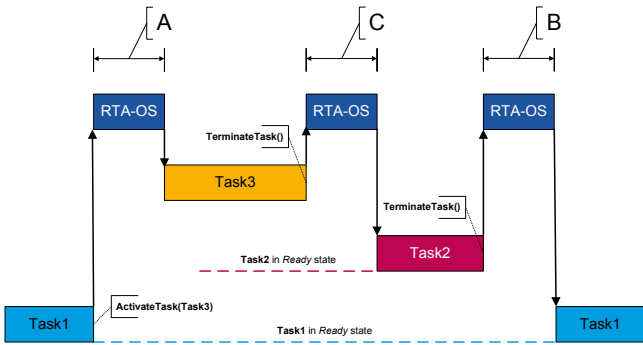


Figure 1 - Task1 is preempted by Task3, followed by a task switch and then normal termination of Task2

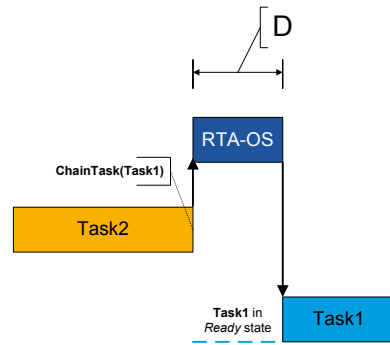


Figure 2 - Task2 chains Task1

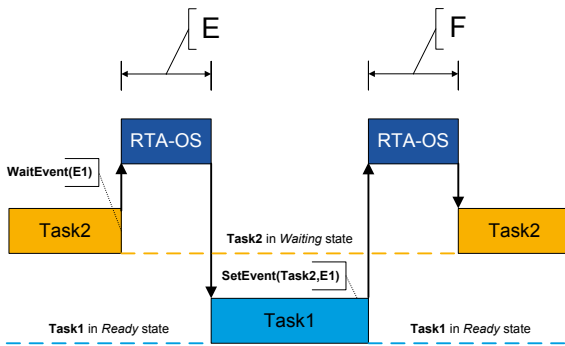


Figure 3 - Task2 waits for an event set by Task1

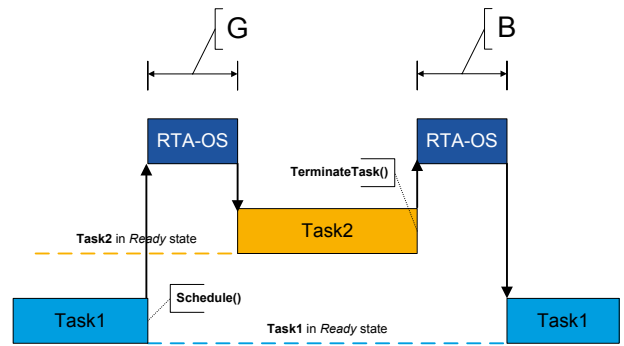


Figure 4 - Task1 allows cooperative scheduling by Task2

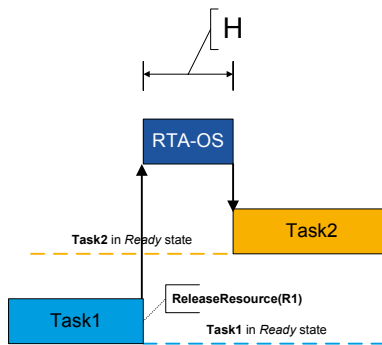


Figure 5 - Task1 releases a resource

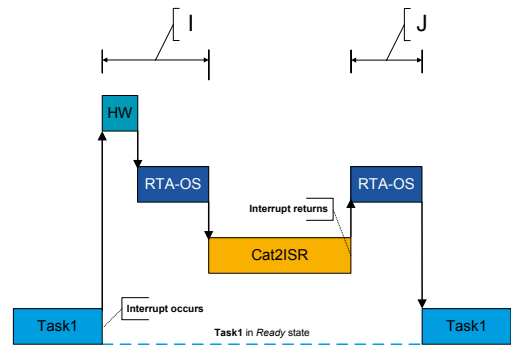


Figure 6 - Category2 ISR entry and exit latency

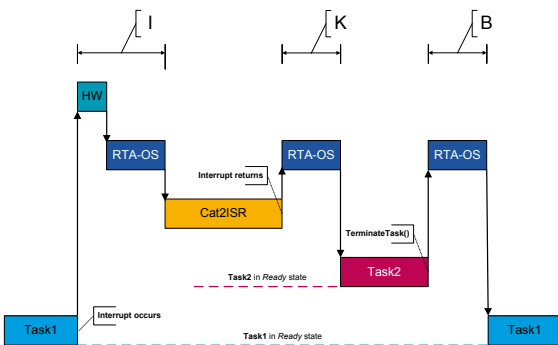


Figure 7 - Category2 ISR switches to Task2

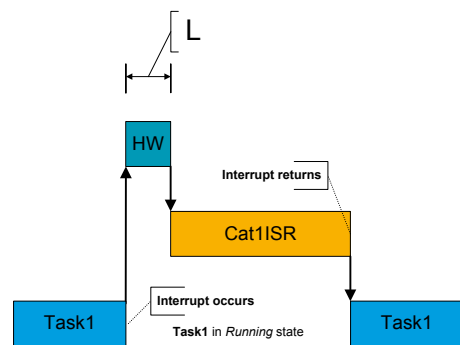


Figure 8 - Category1 ISR entry latency

Order Information

To use RTA-OS it is necessary to purchase a development license for the tools together with an add-on license for the Xilinx Zynq-7000 port. Machine-named, user-named and floating licenses are available.

To use any operating system code generated by RTA-OS in ECU applications, a valid production license is required. Please contact your local ETAS Sales Office for details of production licenses for RTA-OS.

RTA-OS Tools Order Information

Item	Characteristics	Object
F 00K 107 119	Machine-named license for RTA-OS for Windows PC	LD_RTА-OS_VRTA_SC34_LIC-MP
F 00K 107 120	User-named license for RTA-OS for Windows PC	LD_RTА-OS_VRTA_SC34_LIC-UP
F 00K 107 121	Floating license for RTA-OS for Windows PC	LD_RTА-OS_VRTA_SC34_LIC-CP
F 00K 107 136	Product CD for RTA-OS	LD_RTА-OS_VRTA_SC34_PROD

RTA-OS Xilinx Zynq-7000 Port Order Information

Item	Characteristics	Object
F 00K 109 005	Machine-named license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 & 2	ES_RTА-OS_ZYNQRVDS_SC12_LIC-MP
F 00K 109 006	User-named license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 & 2	ES_RTА-OS_ZYNQRVDS_SC12_LIC-UP
F 00K 109 007	Floating license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 & 2	ES_RTА-OS_ZYNQRVDS_SC12_LIC-CP
F 00K 109 008	Machine-named license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 to 4	ES_RTА-OS_ZYNQRVDS_SC34_LIC-MP
F 00K 109 009	User-named license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 to 4	ES_RTА-OS_ZYNQRVDS_SC34_LIC-UP
F 00K 109 010	Floating license for RTA-OS for Xilinx Zynq-7000 Scalability Classes 1 to 4	ES_RTА-OS_ZYNQRVDS_SC34_LIC-CP
F 00K 109 011	Product CD for RTA-OS for Xilinx Zynq-7000	ES_RTА-OS_ZYNQRVDS_PROD

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