RTA-OS PPCe200/GHS Release Note V5.0.32



RTA-OS PPCe200/GHS Release Note - Version 5.0.32 (01-02-2021)



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1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS PPCe200/GHS port plug-in that customizes the RTA-OS development tools for the Freescale/ST MPC5xxx/SPC5xx with the GreenHills compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.0.32 of the RTA-OS PPCe200/GHS plug-in.

1.2 Installation

The installation process is covered in detail in the *PPCe200GHS Port Guide*.



2 Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.



3 Change History

3.1 Version 5.0.32

Additional Features

The following features have been added to this release:

- Support for the cut1.2 SPC584B60 (Chorus1M), SPC584B64 (Chorus1.5M) and SPC584B70 (Chorus2M).
- Support for the GHS compiler 2014.1.9 in addition to previously supported compilers.
- Support for the customer specific GHS compiler 2014.1.9-3fp in addition to previously supported compilers.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.2 Version 5.0.31

Additional Features

The following features have been added to this release:

- Support for the SPC58NH92v2 (Chorus10M).
- Support for the SPC58NH90v2 (Chorus8M) based on the SPC58NH92v2 (Chorus10M).

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.3 Version 5.0.30

Additional Features

The following features have been added to this release:

- Support for the GHS compiler 2020.1.4 in addition to previously supported compilers.
- The target option 'Customer Option Set 4' which when set to true will use a different set of default compiler options. This target option defaults to false.

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No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.4 Version 5.0.29

Additional Features

The following features have been added to this release:

• Full release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.5 Version 5.0.28 (Preview Release)

Additional Features

The following features have been added to this release:

- Support for the MPC5748Cv3 (Calypso6M).
- Support for the MPC5748Cv3_HSM (Calypso6M).
- Support for the SPC574S64 (Sphaero1.5M) based upon the SPC574S60 (Sphaero1M).

Modified Features

The following features have been modified in this release:

 Updates to the MPC5746C, MPC5747Cv2, MPC5746Gv2 and MPC5748Gv2 vector tables.

Removed Features

No features have been removed from this release.



3.6 Version 5.0.27

Additional Features

The following features have been added to this release:

- Support for the MPC5775E based on data sheet only and not tested on real hardware.
- Support for the S32R372 based on data sheet only and not tested on real hardware.

Modified Features

The following features have been modified in this release:

- Updates to the SPC58NH92 (Chorus10M) vector table.
- Caching of the core ID is now mandatory for performance reasons. The old target option 'Cache CoreID' has been replaced by the new option 'Cached CoreID register'.

Removed Features

No features have been removed from this release.

3.7 Version 5.0.26

Additional Features

The following features have been added to this release:

• Support for the SPC584C70 (Chorus2M) based upon the SPC584C74 (Chorus3M).

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.8 Version 5.0.25 (Preview Release)

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

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3.9 Version 5.0.24

Additional Features

The following features have been added to this release:

- Support for the cut 2 MPC5745Rv2 (Rainier 3M) and cut 2 MPC5746Rv2 (Rainier 4M).
- Support for the SPC58NH92 (Chorus10M).

Modified Features

The following features have been modified in this release:

- The example applications now support the MPC5745Rv2 (Rainier 3M) variant.
- In multicore configurations the Category 2 wrapper will now only be emitted for a particular core, if there is a Category 2 interrupt allocated to that core.

Removed Features

No features have been removed from this release.

3.10 Version 5.0.23

Additional Features

- Support for the SPC570S40 based on data sheet only and not tested on real hardware.
- Support for the SPC574S60 based on data sheet only and not tested on real hardware.
- Support for the MPC5606BK based on data sheet only and not tested on real hardware.
- Support for the SPC582B54 (Chorus 768K) based upon the SPC582B60 (Chorus 1M).
- Support for the MPC5745B (Calypso 2M) based upon the MPC5746B (Calypso 3M).
- Initial support for the pre-production SPC58EG84 (Chorus 6M). The hardware we have has three cores but ST confirm the SPC58EG84 will only have two cores and it was this configuration that was tested. ST also inform us that the SPC58EG84 and SPC58NE84 are the same silicon. We note from our hardware that the JTAG ID is 0x11110041 and the contents of the MIDR1 register is 0x58884411, which differ from the SPC58NE84.



The following features have been modified in this release:

• The 'Use Software FP' target option has been replaced by a 'Use Floating Point' target option, which when set to false (default) provides the same functionality and emits '-fnone' but when set to true will emit either '-fsoft' or '-fsingle', which is variant specific.

Removed Features

The following features have been removed from this release:

- Support for the SPC584C.
- Support for the cut 1 MPC5744K and MPC5744K_JDP, SPC574K72 and SPC574K72 JDP.
- Support for the cut 1 MPC5746M and MPC5746M_JDP.
- Support for the cut 1 MPC5777M and MPC5777M_JDP.
- Support for the cut 1 SPC58NE84 and SPC58NE84_JDP.

3.11 Version 5.0.22

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.12 Version 5.0.21 (Preview Release)

Additional Features

- Support for the MPC5604E based on data sheet only and not tested on real hardware.
- Support for the RTA-OS 5.6 EnableInterruptSource and DisableInterruptSource APIs. The ClearPendingInterrupt API is not supported on the PowerPC because it is not feasible to do so.



The following features have been modified in this release:

- Corrected the core type and OS_INTC_x register addresses for the SPC584B (Chorus 2M).
- Clarification: When the 'Generate Cat1 EOIR' target option is disabled, it is permitted to modify the INTC_EOIR register (Or equivalent for Multicore) for category 1 interrupts only.

Removed Features

No features have been removed from this release.

3.13 Version 5.0.20

Additional Features

The following features have been added to this release:

- Support for the GHS compiler 2017.1.4 in addition to previously supported compilers.
- Support MPC5745R (Rainier) based on data sheet only and not tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

The following features have been removed from this release:

• Support for the GHS compilers 2013.5.4, 2014.1.9, 2015.1.4 and 2017.1.2.

3.14 Version 5.0.19 (Preview Release)

Additional Features

- Support for the GHS compiler 2017.1.2 in addition to previously supported compilers.
- Supports trusted-with-protection OS Applications.



The following features have been modified in this release:

• Code for Os_ISRWrapper, Os_RaiseCrossCoreISR and Os_CrossCoreISR has been modified so that each can be placed in separate MemMap sections.

Removed Features

No features have been removed from this release.

3.15 Version 5.0.18

Additional Features

The following features have been added to this release:

- Support SPC58EG80 (Chorus 6M) based on data sheet only and not tested on real hardware.
- Support SPC584C74 (Chorus 4M) based on data sheet only and not tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.16 Version 5.0.17 (Preview Release)

Additional Features

The following features have been added to this release:

- Support for the GHS compiler 2015.1.6 and GHS compiler 2016.5.2 in addition to previously supported compilers.
- Support for the SPC58EC74 (Chorus 3M) and SPC58EC74_JDP (Chorus 3M) based upon the SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively. These have not been tested on real hardware.
- The target option 'Customer Option Set 3' which when set to true will use a different set of default compiler options. This target option defaults to false.

Modified Features

The following features have been modified in this release:

• Relaxed error checking for 'Customer Option Set 2' to allow some options to be set by their respective target option.

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Removed Features

No features have been removed from this release.

3.17 Version 5.0.16

Additional Features

The following features have been added to this release:

 Support for the SPC56EL70 (Leopard) and SPC56HK70 (Komodo) based on the MPC5643L and MPC5675K respectively. These have not been tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.18 Version 5.0.15 (Preview Release)

Additional Features

The following features have been added to this release:

- Version 5.0.15 Preview.
- Tested with the GHS v2015.1.4 compiler and only the MPC5746Mv2, SPC58NE84v2 and SPC58NE84v2_JDP variants.
- Support for the cut 2 SPC58NE84v2 (Eiger 6M) and SPC58NE84v2_JDP (Eiger 6M). Tested on real hardware.
- Support for the SPC58NN84 (Bernina 6M) and SPC58NN84_JDP (Bernina 6M). These have not been tested on real hardware.

Modified Features

- All SPC58xx84 (Eiger 6M) variants have been renamed to SPC58NE84 in order to differentiate from the SPC58NN84 (Bernina 6M).
- Updates to the cut 1 SPC58NE84 and SPC58NE84_JDP vector table.
- Syscall refactored and renamed to reduce the number of instructions.
- The example applications now support the MPC5746Mv2, MPC5777Mv2, SPC574K72v2, SPC582B60, SPC58EC80, SPC58NE84 and SPC58NE84v2 variants.



Removed Features

No features have been removed from this release.

3.19 Version 5.0.14

Additional Features

The following features have been added to this release:

• Support for the SPC582B50 (Chorus 512K), SPC58EC70 (Chorus 2M) and SPC58EC70_JDP (Chorus 2M) based upon the SPC582B60 (Chorus 1M), SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively.

Modified Features

The following features have been modified in this release:

• Variants MPC5673Fv2 and MPC5674Fv2 now utilize the instructions within the 'Volatile Context Save/Restore APU'.

Removed Features

No features have been removed from this release.

3.20 Version 5.0.13

Additional Features

The following features have been added to this release:

• Version 5.0.13 Preview.

Modified Features

The following features have been modified in this release:

• Corrects support for the SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M). Tested on real hardware.

Removed Features

No features have been removed from this release.



3.21 Version 5.0.12

Additional Features

The following features have been added to this release:

- Version 5.0.12 Preview.
- Support for the SPC582B60 (Chorus 1M).
- Support for the SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M). These have not been tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.22 Version 5.0.11

Additional Features

The following features have been added to this release:

- Version 5.0.11 Preview.
- Support for the GHS compiler 2015.1.4 in addition to previously supported compilers.
- Experimental support for the SPC582B60 (Chorus 1M).
- The target option 'Customer Option Set 2' which when set to true will use a different set of default compiler options. This target option defaults to false.
- The target option 'Optimizer Setting' which offers optimizer settings of Osize otherwise defaulting to Ospeed.
- Disables warnings of GHS warning 667 in OS header files.

Modified Features

No features have been modified in this release.

Removed Features

The following features have been removed from this release:

• Support for the cut 1 MPC5673F, cut 1 MPC5674F and SPC582B.



3.23 Version 5.0.10

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

• Testing of the 'Customer Option Set 1' options and compiler patches has been extended to other supported variants.

Removed Features

No features have been removed from this release.

3.24 Version 5.0.9

Additional Features

The following features have been added to this release:

- The target option 'Customer Option Set 1' which when set to true will use a different set of default compiler options. This target option defaults to false.
- GHS 2014.1.9 compiler patches 8614, 9045 and 9127 were used and tested against.
- Testing of the 'Customer Option Set 1' options and compiler patches was limited to the MPC5643L variant.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.25 Version 5.0.8

Additional Features

- Support for the MPC5746B (Calypso 3M) and MPC5746C (Calypso 3M). These have not been tested on real hardware.
- The GHS __memory_changed() memory barrier optimization intrinsic function has been placed around other intrinsic functions to prevent instruction re-ordering.
- The target option 'Always call GetAbortStack' to always use Os_Cbk_GetAbortStack() to set up a safe area of memory to use as a stack when executing the ProtectionHook.



The following features have been modified in this release:

- Corrected multicore support for the MPC5746Gv2 and MPC5747Cv2.
- Updated the default implementation of Os_Cbk_GetAbortStack() so that no stack is used in both single and multicore applications.
- The code to support the 'enable stack repositioning' target option has been updated. The assembly language instructions generated now do not rely on values stored in the CPU general purpose registers to be preserved over the call to untrusted code.

Removed Features

No features have been removed from this release.

3.26 Version 5.0.7

Additional Features

The following features have been added to this release:

• Support for the GHS compiler 2014.1.9. Maintains support for the GHS compiler 2013.5.4.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.27 Version 5.0.6

Additional Features

The following features have been added to this release:

- Version 5.0.6 Beta.
- Support for the cut 2 MPC5746Gv2 (Calypso 3M) and cut 2 MPC5747Cv2 (Calypso 4M).

Modified Features

The following features have been modified in this release:

• Standardized naming convention for 'Software Interrupt x' vectors.

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Removed Features

No features have been removed from this release.

3.28 Version 5.0.5

Additional Features

The following features have been added to this release:

- Supports Eiger chip, SPC58xx84 and SPC58xx84_JDP.
- Update for RTA-OS 5.4 compatibility
- Added the Os_IntChannel_x macro
- Target option: 'Cache CoreID'. e.g. for the Eiger, using '-target_option:Cache CoreID=PMGCO' will significantly improve performance, especially with untrusted code, because the Core ID is cached in the Performance Monitoring unit. This means that OS APIs can discover which core is running much faster. Other devices will be able to cache the Core ID in a SPRG register, but this is not possible on the Eiger. The Performance Monitoring unit cannot be used when this option is in effect.
- Target option: 'OS Locks disable Cat1'. This can be used to specify that all interrupts are disabled while internal OS spinlocks are held. This does not affect spinlocks accessed using the GetSpinlock or TryToGetSpinlock APIs.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.29 Version 5.0.4

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

• Reduced library build time.

Removed Features

No features have been removed from this release.



3.30 Version 5.0.3

Additional Features

The following features have been added to this release:

- Version 5.0.3 Beta.
- Support for the MPC5748Gv2 (Calypso6M).
- Support for the MPC5748GCompatibility variant which shares the common interrupt vectors from the cut 1 and cut 2 MPC5748G devices.
- Initial support for the SPC584C (Chorus4M), SPC584B (Chorus2M) and SPC582B (Chorus1M). This is based solely upon the initial documentation and has not been tested on real hardware.
- Initial support for the MPC5746R (Rainier). This has not been tested on real hardware.

Modified Features

The following features have been modified in this release:

- The software semaphore implementation now uses 32 bit decorated storage instructions instead of 8 bit versions.
- Improvements to winIDEA ORTI and signalling to Profiler.
- Optimized instructions used in both 32 and 64 bit implementations of Os_setjmp/Os_longjmp.

Removed Features

The following features have been removed from this release:

• Support for the cut 1 MPC5748G.

3.31 Version 5.0.2

Additional Features

The following features have been added to this release:

• Support for the cut 2 MPC5746Mv2 (McKinley) and JDP variant.

Modified Features

No features have been modified in this release.



Removed Features

No features have been removed from this release.

3.32 Version 5.0.1

Additional Features

The following features have been added to this release:

- Version 5.0.1 Beta.
- Support for the MPC5777C (Cobra55) and MPC5645S (Spectrum).
- Support for the cut 2 MPC5744K/SPC574K72 and JDP variants.
- For the cut 2 Matterhorn (MPC5777Mv2 and MPC5777Mv2_JDP), single writes to OS_INTC_CPR are used. (The cut 1 version needs double writes as an erratum workaround.)
- Support for the MPC5777Mv2_HSM (Matterhorn).
- The target option 'Generate Cat1 EOIR' has been added to emit code to write to the EOIR register in Category 1 ISRs.

Modified Features

The following features have been modified in this release:

- Updates to cut 1 MPC5777M vector table.
- Support for using the 'Volatile Context Save/Restore APU'. RTA-OS uses the APU for non-rfi based IVOR interrupts. Otherwise for all other Category 1 ISRs support is provided by the compiler.
- Workaround added for software vectoring with MPC57xx devices. Priority inversion could occur with Category 2 ISRs.
- The placement of Crosscore ISRs, Category 2 Os_wrapper and Spinlock functions into a CODE_FAST section (See Os_MemMap.h).

Removed Features

No features have been removed from this release.

3.33 Version 5.0.0

Additional Features

The following features have been added to this release:

• Support for the MPC5744P (Panther).



No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.34 Version 4.9.0

Additional Features

The following features have been added to this release:

- Multicore support.
- Support for the GHS compiler 2013.5.4.
- Support for many new variants.
- The target option 'Block default interrupt' has been added to set all unused interrupts to disabled with a default interrupt handler on the lowest priority.
- The target option 'ORTI Stack Fill' has been added to support debugger calculation of application stack usage using the ORTI details.
- Adds target option to select software vectoring rather than hardware vectoring for dispatching INTC interrupts. RTA-OS will supply the software dispatcher unless you configure your own Category 1 handler on IVOR4, in which case you can implement the software dispatcher yourself as a standard Category 1 ISR. For software vectoring, the Os_INTC_vectors table contains pointers to functions that take a uint32 argument that is the vector number, so you can use 'Os_INTC_vectorsvector;' to perform the dispatching.
- Supports 'Enable stack repositioning' option
- ORTI support for Category 1 ISRs in multicore configurations.
- SRRx registers for the save/restore context are now also emitted for the Critical, Watchdog, MachineCheck and Debug IVOR interrupts.
- Support for the Performance Monitor Interrupt (IVOR 35) on z7 cores.
- Additional support for using a software semaphore instead of the SEMA4 hardware. The software semaphore option is only applicable to MPC57xx variants.

Modified Features

The following features have been modified in this release:

• Slight timing adjustment in software vectoring code for Cat2 ISRs, advised by Freescale. Without it interrupts raised via the SWT bit in a PSR might get missed.



Removed Features

The following features have been removed from this release:

• Support for the MPC5514 and MPC5516.

3.35 Version 2.0.21

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.36 Version 2.0.20

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.37 Version 2.0.19

Additional Features

The following features have been added to this release:

- Version 2.0.19 Preview
- Support for SPE context handling within RTA-OS

Modified Features

- RTA-OS using VLE instruction code (linkable with non-VLE).
- IPL max is now always 16.
- Version v5.2.4 of the GHS toolchain is now the only supported version.



Removed Features

No features have been removed from this release.

3.38 Version 2.0.10

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.39 Version 2.0.8

Additional Features

The following features have been added to this release:

- Version 2.0.8 Preview 1
- Configured INTC vectors can now be disabled and re-enabled through the macros defined in Os_DisableInterrupts.h.

Modified Features

The following features have been modified in this release:

- Corrected a couple of comments in the vector generation code.
- Os_isr_count is no longer accessed using the SDA.

Removed Features

No features have been removed from this release.

3.40 Version 2.0.7

Additional Features

The following features have been added to this release:

• Version 2.0.7 Preview 1



The following features have been modified in this release:

- Corrected ORTI generation whereby the ';' symbol was missing from the CUR-RENTAPPLICATION statement.
- Stack corruption testing in ISRs is now fully tested and working target option.

Removed Features

No features have been removed from this release.

3.41 Version 2.0.6

Additional Features

The following features have been added to this release:

- Version 2.0.6 Preview 1
- Support for aligning stack to MPU regions in tasks and ISRs.
- Stack corruption testing in ISRs. However, the target option should not be used because it hasn't been fully tested.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.42 Version 2.0.5

Additional Features

- A target option 'Use Short Enum' has been added that when set to 'true' will use the '-short_enum' compiler option. The default option is 'false', thus using the '-no short enum' compiler option.
- The following compiler options have been added for use in user code: '-bsp=generic', '-checksum', '-delete', '-no_ignore_debug_references', 'no_commons', '-Wundef', '-relative_xof_path', '-preprocess_assembly_files', '-inline_prologue', '-Ospeed'.



The following features have been modified in this release:

• Corrected occurrences of '-fnone' appearing in addition to '-fsoft' in the compilation options for user code when target option 'Use Software FP' is defined.

Removed Features

No features have been removed from this release.

3.43 Version 2.0.4

Additional Features

The following features have been added to this release:

- Version 2.0.4 Preview 1
- Added additional variants MPC5675K, MPC5644B, MPC5644C, MPC5645B, MPC5645C, MPC5646B and MPC5646C as single core devices and using the most appropriate matching -cpu option.

Modified Features

The following features have been modified in this release:

• Corrected code to initialize the IVPR when supporting 4Kbyte aligned vector tables.

Removed Features

No features have been removed from this release.

3.44 Version 2.0.3

Additional Features

No features have been added to this release.

Modified Features

- Version 5.1.7 of the GHS toolchain is now additionally supported.
- Variants SPC560C and MPC5604C use the compiler option -cpu=ppc5534. Remaining variants use the most appropriate matching -cpu option.
- Code to initialize the IVPR now supports 20 bits in addition to 16 bits. Thus allowing the vector table to be additionally 4Kbyte aligned.



- A target option 'Use Software FP' has been added that when set to 'true' will use the '-fsoft' compiler option. The default option is 'false', thus using the '-fnone' compiler option.
- The generic 'Platform_types.h' file now configures the 'float32' and 'float64' variables of type 'float' and 'double' respectively if the 'Use Software FP' target option is set to 'true'. The default types are 'int' and 'int'.

Removed Features

No features have been removed from this release.

3.45 Version 2.0.2

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- The assembly source code for interrupt vectors has been modified to use up-to-date function decorations.
- Add some previously missed variant-specific interrupt sources and give default names to interrupts which are nominally not present on a variant.

Removed Features

No features have been removed from this release.

3.46 Version 2.0.1

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.47 Version 2.0.0

Additional Features

No features have been added to this release.

Modified Features

No features have been modified in this release.

If printed, this document is an uncontrolled copy.



Removed Features

The following features have been removed from this release:

• Removed variants MPC5643, JPC563M, JPC560P.

3.48 Version 1.99.4

Additional Features

The following features have been added to this release:

• Added additional variants MPC5604S, MPC5607B, MPC5674F.

Modified Features

The following features have been modified in this release:

• Regularized the capitalization of the interrupt vector names.

Removed Features

The following features have been removed from this release:

• Removed variant MPC5607

3.49 Version 1.99.2

Additional Features

The following features have been added to this release:

• Beta release. SC1/2/3/4 implemented.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.50 Version 1.0.0

Additional Features

The following features have been added to this release:

 Supports variants: MPC5516z1, MPC5516z0, SPC563M, MPC5514z1, MPC5514z0, MPC5534, MPC5553, MPC5554, MPC5561, MPC5565, MPC5566, MPC5567, SPC560P, SPC560B, SPC560C, SPC560S



The following features have been modified in this release:

• The interrupt naming scheme has been updated to match the style used in the processor documentation

Removed Features

No features have been removed from this release.

3.51 Version 0.9.3

Additional Features

The following features have been added to this release:

• Beta release with SPS563M and MPC5516z1

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.52 Version 0.9.2

Additional Features

The following features have been added to this release:

• Initial alpha release

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.



4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

4.1 Version 5.0.28 (Preview Release)

EHI 634466

Status:	Fixed
Title:	The FlexRay vectors were incorrectly present on the
	SPC574S60.
Description:	On the SPC574S60 the FlexRay interrupt vector entries
	should not be present in the interrupt vector table.

4.2 Version 5.0.27

EHI 620776						
Status:	Fixed					
Title:	Untrusted stack check functionality not working.					
Description:	In versions 5.0.15 to 5.0.26, the target option "Untrusted					
	stack check" did not properly switch into untrusted mode					
	to check the stack validity. The detection of an invalid					
	stack might be delayed as a consequence.					

EHI 633474

Status:	Fixed							
Title:	Incorrect	compiler	сри	option	was	used	for	the
	MPC5744	v2/SPC574	1K72v2	2.				
Description:	The	MPC574	4Kv2/	MPC574	4Kv2_	JDP		and
SPC574K72v2/SPC574K72v2_JDP variants used								the
	incorrect compiler cpu option. The correct cpu option							
	-cpu=ppc	5744kz410						

4.3 Version 5.0.26

EHI 614350	
Status:	Fixed
Title:	No SPE register saving when using software vectoring.
Description:	The 'Preserve SPE' target option was not being considered
	when 'Use software vectoring' was TRUE. The SPE/EFPU2
	related registers were not being saved and restored in the
	software vectoring handler.



EHI 614352

Status:	Fixed
Title:	Clarification of EOIR handling.
Description:	The documentation has been improved to explain that
	Category 1 ISRs should not write EOIR when using soft-
	ware vectoring. EOIR should be written by Category 1 ISRs
	in hardware vectoring mode, but the 'Generate Cat1 EOIR'
	target option can be used to make this automatic.

4.4 Version 5.0.25 (Preview Release)

EHI 612099	
Status:	Fixed
Title:	Incorrect time and stack measurements - software vector- ing.
Description:	The issue described in EHI 598675 was only fixed for hard- ware interrupt vectoring configurations. This version cor- rects the same issue in the software vectoring configura- tions.

EHI 613026

Fixed
Incorrect time and stack measurements - multicore.
The issue described in EHI 598675 was only fixed for
single-core configurations. This version corrects the same
issue in the cross-core interrupt handler.

EHI 613034

Status:	Fixed
Title:	Incorrect cross-core interrupt behavior.
Description:	A line of code to disable global interrupts was being condi-
	tionally emitted in the cross-core interrupt when it should
	have been unconditionally emitted.

4.5 Version 5.0.24

EHI 598675	
Status:	Fixed
Title:	Incorrect time and stack measurements
Description:	It was possible for a Category 2 interrupt to pre-empt an-
	other Category 2 interrupt just before it had completed
	calculating time and stack values for the code that it had
	pre-empted. This could result in miscalculation of these
	values.

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EHI 598676

Status:FixedTitle:Failure to disable/restore MPU in interrupts when Trusted-
WithProtection OS Applications exist

Description: The MPU has to be enabled and disabled appropriately to support TrustedWithProtection on the PowerPC. Category 2. The code to do this was omitted in the Category 2 interrupt and cross-core interrupt handlers. This could result in the handler code wrongly running with the MPU enabled, which might result in incorrect memory traps. Alternatively it could result in the MPU being disabled when returning to pre-empted code.

EHI 609582

Status:	Fixed							
Title:	No	library	bu	ilt	wh	ien i	using	the
	MPC5	744Kv2/MI	PC5744	ا_Kv2	DP			and
	SPC57	/4K72v2/S	PC574K	72v2_	JDP.			
Description:	The	library	will	fail	to	build	wher	า us-
	ing	the	MPC5	744K	v2/MI	PC5744K\	/2_JDP	or
	SPC57	/4K72v2/S	PC574K	72v2_	JDP	because	their	shared
	regist	er definitio	on entrie	es wer	re mis	ssing.		

4.6 Version 5.0.23

EHI 584356	
Status:	Fixed
Title:	Possible incorrect return address for ECC tasks that termi- nate.
Description:	If an ECC task terminates by returning from the task body or calling TerminateTask() with lightweight termination ac- tive, the return address could be incorrect and cause a crash. ECC Tasks that only loop on WaitEvent and do not terminate are not affected.
EHI 587531	
Status:	Fixed
T !+1 -	In some stills at some some the MDCE74ED and MDCE74CD

Title:	Incorrect boot core on the MPC5745R and MPC5746R.
Description:	The boot core on the MPC5745R and MPC5746R was incor-
	rectly implemented as chip core 0 but should be chip core
	1 (Autosar core 0).



EHI 591180

Fixed
Configuring trusted-with-protection with SC1/SC2
Previously when trusted-with-protection and SC1 or SC2
was configured, the code generated was incorrect and re-
sulted in a compilation error.

4.7 Version 5.0.21 (Preview Release)

EHI 577518

Status:	Fixed
Title:	Exception occurs in an untrusted OS application when "En-
	able stack repositioning" is enabled.
Description:	The exception is caused by a write to an OS variable which
	can not be accessed once in untrusted mode. Only Tools
	5.5.6+ and target v5.0.19+ are affected.

EHI 580078

Status:	Fixed
Title:	Incorrect compiler cpu option was used for the SPC584B.
Description:	The supported GHS compilers up to 2017.1.4 do not
	specifically provide a -cpu option to support the SPC584B
	variant. The option originally used was incorrect. It is now
	based on the closest variant with a matching core type.

EHI 580179

Status:	Fixed
Title:	Use of xAllInterrupts APIs before StartOS() with "Cache
	CoreID" enabled.
Description:	AUTOSAR states that the DisableAllInterrupts(), En-
	ableAllInterrupts() and SuspendAllInterrupts(), Re-
	sumeAllInterrupts() APIs can be used before StartOS() is
	called. However with CoreID caching enabled the cached
	CoreID register had not yet been initialized.

4.8 Version 5.0.20

EHI 564983	
Status:	Fixed
Title:	Incorrect value applied to the INTC_BCR register for hard-
	ware vectoring on the MPC5745R and MPC5746R.
Description:	An incorrect value was written to the INTC_BCR register,
	resulting in hardware vectoring only applying to Autosar
	core 0. Only the MPC5745R and MPC5746R were affected.



4.9 Version 5.0.18

EHI 549913	
Status:	Fixed
Title:	Crash caused by stack misalignment in ISRs when "Enable stack repositioning" was used with memory protection but the "Enable untrusted stack check" option was false.
Description:	Applies only to RTA-OS 5.4.4 to 5.5.3. The ISR handler would not reset the stack after adjusting it to run the ISR. The workaround is to set "Enable untrusted stack check" option to true.
EHI 550151	
Status:	Fixed
Title:	Compilation failure with memory protection but without "Enable stack repositioning" option enabled
Description:	In configurations that supported the forced termination of ISRs, a compilation failure could occur if memory protec- tion was active but option 'Enable stack repositioning' was false.

4.10 Version 5.0.16

EHI 525915	
Status:	Fixed
Title:	Preserve SPE target option and the SPE bit in some Cate-
Description:	The SPE bit in some Category 1 interrupts was not re- enabled if the 'Preserve SPE' target option is enabled, nor was the variant specific SPE context saved or restored.
EHI 528584	
Status:	Fixed
Title:	Raw interrupts text

nuc.	
Description:	Description of raw interrupt functionality added, whereby
	if an IVOR vector name is prefixed with 'b_' it allows the
	user to provide their own handler, as opposed to an RTA-
	OS generated handler.



4.11 Version 5.0.15 (Preview Release)

EHI 522336	
Status:	Fixed
Title:	Compiler optimization affecting ordering of instructions around INTC_CPR writes
Description:	In some configurations, the GHS v2013.5.4, v2014.1.9 and v2015.1.4 compilers could optimize the output assembler such that a variable that was updated in the C code just before a write to INTC_CPR, would actually get updated just after it. This could cause problems when lowering the interrupt priority. The GHSmemory_changed() memory barrier has been applied to INTC_CPR writes to prevent this behavior.

4.12 Version 5.0.12

EHI 500989	
Status:	Fixed
Title:	Incorrect MPC5744P vector table entry
Description:	Interrupt vector 379 was considered a valid vector but is
	in fact reserved and not selectable. Interrupt vector 622
	was duplicated, thus meaning vector 623 was missing.

EHI 501213

Status:	Fixed
Title:	Possible register corruption
Description:	It is possible for register corruption to occur in the Call-
	TrustedFunction API function when it is used to call un-
	trusted functions (an RTA-OS extension to AUTOSAR) and
	the code in the untrusted function corrupts registers. This
	will only occur if memory protection and stack realign-
	ment is enabled. This occurs on versions of the port before
	5.0.8.

xed

- *Title:* Possible stack location swapped for Autosar cores 1 and 2 on 3 core JDP variants
- Description: On the variants MPC5746M_JDP, MPC5746Mv2_JDP, MPC5777M_JDP, MPC5777Mv2_JDP and SPC58xx84_JDP it is possible that the generated example multicore start up code swaps the respective stack location for Autosar cores 1 and 2. The effect of this can lead to errors being reported on the wrong core and/or possible data corruption leading to a machine check exception. Port versions before 5.0.10 are affected by this issue.



4.13 Version 5.0.11

EHI 485207 <i>Status:</i> <i>Title:</i> <i>Description:</i>	Fixed Os_GetAbortStack buffer overflow On the K2 (all MPC5744K, all SPC574K72) and Calypso 4M (MPC5747Cv2) devices only, with the default implemen- tation of Os_GetAbortStack, there will be an overflow if 'abortstack' is called on hardware core 2.
EHI 495712	
Status:	Fixed
Title:	Example code for Os_Cbk_GetAbortStack might return NULL
Description:	This occurs in configurations that use the Os_Cbk_SetMemoryAccess callback to update the memory protection settings for untrusted code, but where the stack value is not actually passed to the callback. i.e. Stack Monitoring is disabled AND target option 'Enable stack repositioning' is false a NULL value can be returned.

4.14 Version 5.0.9

EHI 472958 Status: Title: Description:	Fixed Os_Enable_ macros in Os_DisableInterrupts.h The macros generated in Os_DisableInterrupts.h for the MPC5643L, MPC5675K and SPC58xx84 parts were incor- rect. They did not take account of the second INTC.
EHI 480160	
Status:	Fixed
Title:	Backwards compatibility between Tools v5.4.3 and Tools v5.4.2
Description:	ISR termination code generated by the target produced a compilation error in Os_Wrapper.c when using Tools v5.4.2 that was not present when using Tools v5.4.3.
/ersion 5.0.8	

4.15 Version 5.0.8

EHI 464449	
Status:	Fixed
Title:	Preserve SPE target option text
Description:	Improved clarity with regard to how this target option re-
	lates to the compiler and variant in use.



4.16 Version 5.0.5

EHI 448937	
Status:	Fixed
Title:	Terminating ECC tasks with the Enable stack repositioning option
Description:	If an interrupt occurred during the execution of the heavy- weight version of TerminateTask for an ECC task, the setjmp/longjmp buffer used to return to the OS could be- come corrupted and cause unpredictable behavior. Note that ECC tasks do not normally terminate, so this should not be a common use-case.
EHI 450615	
Status:	Fixed

Status:	Fixed
Title:	Enable untrusted stack check
Description:	The 'Enable untrusted stack check' in the interrupt han-
	dler was checking the preempted stack for both trusted
	and untrusted code. It should only have checked when
	it was preempting untrusted code, because the check
	switches briefly to untrusted mode. The stack might have
	been in a legal trusted area, but not a legal untrusted
	area. This could have caused a spurious protection trap,
	depending on the memory protection settings used.

4.17 Version 5.0.4

EHI 437256	
Status:	Fixed
Title:	Possible overstated stack use.
Description:	In configurations with stack monitoring enabled, a cate-
	gory 2 ISR pre-empting another ISR could cause the stack
	usage of the pre-empted task to appear to be higher than
	it should be. This is because some of the stack used by
	the pre-empted ISR was getting added to the task stack
	usage.

Status:	Fixed
Title:	Early Task execution.
Description:	On pre MPC57xx and MPC5777C variants that use the
	Os_isr_count variable to cope with a race condition in the
	INTC, configurations that enable stack or execution mon-
	itoring could run a task activated in a pre-empting cate-
	gory 2 ISR sooner than normal. The task should only run
	when the lowest priority ISR completes.



4.18 Version 5.0.3

EHI 437404	
Status:	Fixed
Title:	Os_InitializeVectorTable
Description:	Os_InitializeVectorTable fails to disable all Category 2 in- terrupts via the OS_INTC_CPRx register for a core ID greater than 1. Thus only 3 core variants were affected.
Version 5.0.1	
EHI 403742	Fixed
Status.	Theorem 1997

Status:	Fixed
Title:	Additional winIDEA ORTI instrumentation to Terminate-
	Task.
Description:	

4.20 Version 2.0.2

4.19

EHI 96602

<i>Status:</i>	Fixed
Title:	Cat2 ISRs
Description:	When a resource was shared between a task and an ISR then it was possible to get an extra task dispatch due to a race condition when raising the IPL to OS level whilst the resource is locked.

4.21 Version 2.0.1

СПІ 91244	EHI	91244	
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Status:	Fixed
Title:	Category 1 ISRs
Description:	For certain configurations, the CAT1_ISR wrapper could
	enable interrupts again before SRR0/1 context was saved

4.22 Version 1.0.0

EHI 85620	
Status:	Fixed
Title:	Target-specific parameters not saved
Description:	It was possible to set some target-specific parameters in the GUI that would not be restored from disk.

Status:	Fixed
Title:	Os_OrtiApiID
Description:	<code>Os_OrtiApiID</code> type was <code>OS_OrtiIdType</code> and should be
	Os_OrtildType.



EHI 85720

Status:	Fixed
Title:	ORTI generation
Description:	ORTI generation would fail in systems with no tasks

EHI 85721

Status:	Fixed
Title:	Counters and ECC-only actions
Description:	Counter code was faulty if alarms/expiries only set events.
	The counter would not advance.

Status:	Fixed
Title:	Misra deviation 12.10
Description:	Misra deviation 12.10 was reported as Misra deviation
	12.1



5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation None. Workaround None.

5.2 PPCe200GHS DLL

There are the following limitations for this tool:

Limitation When the '-fsoft' or '-fsingle' compiler option is used (via the 'Use Floating Point' target option), then the code generated by the compiler for CAT1_ISRs does not save and restore the SRR0/1 registers. You should ensure that your CAT1 ISR handlers do not change the content of these registers.

Workaround None.

- **Limitation** If a multicore variant does not enforce data coherency in hardware when the D-CACHE is enabled, then any data shared between cores has to use software mechanisms to flush/invalidate the cache. It is not currently clear how to do this efficiently in an AUTOSAR implementation.
- **Workaround** Do not enable D-CACHE.
- LimitationRemember that if you call Os_TimingFaultDetected from a Timing
Protection interrupt, the interrupt handler will not exit normally so
you will need perform EOIR directly in your handler.
- Workaround None.
- Limitation The MPC5748GCompatibility variant amalgamates the common interrupt vectors from the cut 1 and cut 2 silicon revisions and also facilitates the ability to run code on both silicon revisions. Note: the restriction on core 2 of cut 1 devices that hardware vectoring can not be used and that on cut 2 devices the clock dividers have changed.
 Workaround To fully utilize cut 2 silicon please use the MPC5748Gv2 variant.
- LimitationThe MPC5644C, MPC5645C and MPC5646C are only supported as a
single core variant, specifically the z4d core.
- Workaround None.
- Limitation The RTA-OS 5.6 ClearPendingInterrupt API is not supported on the PowerPC because it is not feasible to do so. The API will return E_OS_ID for all ISRs.
- Workaround None.

RTA-OS PPCe200/GHS Release Note V5.0.32

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Limitations



6 **Contacting ETAS**

6.1 **Technical Support**

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see below).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The command line (or reproduction of steps) that result in an error message
- The error messages or return codes you received (if any)
- Your .xml, .arxml and .rtaos files
- The file Diagnostic.dmp if it was generated

6.2 **General Enquiries**

6.2.1 **ETAS Global Headquarters**

ETAS GmbH Borsigstrasse 24 70469 Stuttgart Germany

Phone: WWW:

+49 711 3423-0 +49 711 3423-2106 www.etas.com

6.2.2 ETAS Local Sales & Support Offices

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

Fax:

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