RTA-OS PPCe200/HighTec

Release Note - Version 5.0.24 (28-08-2019)

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Safety Notice

This ETAS product fulfills standard quality management requirements. If requirements of specific safety standards (e.g. IEC 61508, ISO 26262) need to be fulfilled, these requirements must be explicitly defined and ordered by the customer. Before use of the product, customer must verify the compliance with specific safety standards.

Contents

1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS PPCe200/HighTec port plug-in that customizes the RTA-OS development tools for the Freescale/ST MPC5xxx/SPC5xx with the HighTec compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.0.24 of the RTA-OS PPCe200/HighTec plug-in.

1.2 Installation

The installation process is covered in detail in the *PPCe200/HighTec Port Guide*.

2 Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.

3 Change History

3.1 Version 5.0.24

Additional Features

The following features have been added to this release:

- Support for the SPC584C70 (Chorus2M) based upon the SPC584C74 (Chorus3M).
- Support for the SPC58NH92 (Chorus10M).

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.2 Version 5.0.23

Additional Features

The following features have been added to this release:

- Support for the SPC582B54 (Chorus 768K) based upon the SPC582B60 (Chorus 1M).
- Support for the MPC5745B (Calypso 2M) based upon the MPC5746B (Calypso 3M).
- Support for the cut 2 MPC5745Rv2 (Rainier 3M) and cut 2 MPC5746Rv2 (Rainier 4M).
- Support for the S32R274 (RaceRunner Ultra) based upon the MPC5775K (RaceRunner).
- Initial support for the pre-production SPC58EG84 (Chorus 6M). The hardware we have has three cores but ST confirm the SPC58EG84 will only have two cores and it was this configuration that was tested. ST also inform us that the SPC58EG84 and SPC58NE84 are the same silicon. We note from our hardware that the JTAG ID is 0x11110041 and the contents of the MIDR1 register is 0x58884411, which differ from the SPC58NE84.
- The example applications now support the MPC5745Rv2 (Rainier 3M) variant.

Modified Features

The following features have been modified in this release:

- A Category 1 interrupt placed on the IVOR vectors will not have its respective SRRx register pair saved or restored, except in the case of IVOR_4 (External Interrupt) for software vectoring, (IVOR_10 (Decrementer) and IVOR_11 (Fixed Interval Timer) if present) which can be pre-empted and therefore must have their SRRx register pair saved and restored.
- In multicore configurations the Category 2 wrapper will now only be emitted for a particular core, if there is a Category 2 interrupt allocated to that core.

Removed Features

No features have been removed from this release.

3.3 Version 5.0.22 (Preview Release)

Additional Features

The following features have been added to this release:

- Support for the MPC5604E based on data sheet only and not tested on real hardware.
- Support for the MPC5606BK based on data sheet only and not tested on real hardware.
- Support for the SPC570S40 based on data sheet only and not tested on real hardware.
- Support for the SPC574S60 based on data sheet only and not tested on real hardware.
- Support for the RTA-OS 5.6 EnableInterruptSource and DisableInterruptSource APIs. The ClearPendingInterrupt API is not supported on the PowerPC because it is not feasible to do so.

Modified Features

The following features have been modified in this release:

- Corrected the core type and OS_INTC_x register addresses for the SPC584B (Chorus 2M).
- Clarification: When the 'Generate Cat1 EOIR' target option is disabled, it is permitted to modify the INTC_EOIR register (Or equivalent for Multicore) for category 1 interrupts only.

Removed Features

The following features have been removed from this release:

- Support for the SPC584C.
- Support for the cut 1 MPC5744K and MPC5744K_JDP, SPC574K72 and SPC574K72_JDP.
- Support for the cut 1 MPC5746M and MPC5746M_JDP.
- Support for the cut 1 MPC5777M and MPC5777M_JDP.
- Support for the cut 1 SPC58NE84 and SPC58NE84_JDP.

3.4 Version 5.0.21

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Tuned SEMA4 handling code based on testing on the MPC5775K (RaceRunner).

Removed Features

No features have been removed from this release.

3.5 Version 5.0.20 (Preview Release)

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Updated support for the MPC5775K (RaceRunner), including testing on real hardware.
- The 'Preserve SPE' target option is used to preserve SPE-related registers when preemption occurs. From this version onwards, the OS checks the MSR[SPE/SPV] bit to decide whether to preserve the appropriate registers. They are only preserved if it is set. This means that on devices such as the MPC5775K (where not all cores support SPE) it is now possible to control which cores use register preservation. It is normal for application code to initialize the SPE bit appropriately for each core before calling StartOS() and then not modify it afterwards. The OS will ensure that MSR[SPE] is preserved when interrupts or exceptions occur.

Removed Features

No features have been removed from this release.

3.6 Version 5.0.19 (Preview Release)

Additional Features

The following features have been added to this release:

- Initial support for the MPC5775K (RaceRunner). The MPC5775K has been partially tested on real hardware.
- Software semaphores on the MPC5775K (RaceRunner) are not supported in this preview.
- SPE support for the MPC5775K (RaceRunner) is not fully supported in this preview.
- Support SPC58EG80 (Chorus 6M) based on data sheet only and not tested on real hardware.
- Support SPC584C74 (Chorus 4M) based on data sheet only and not tested on real hardware.
- Support for the SPC58EC74 (Chorus 3M) and SPC58EC74_JDP (Chorus 3M) based upon the SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively. These have not been tested on real hardware.
- Supports trusted-with-protection OS Applications.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.7 Version 5.0.18 (Preview Release)

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Code for Os_ISRWrapper, Os_RaiseCrossCoreISR and Os_CrossCoreISR has been modified so that each can be placed in separate MemMap sections.

Removed Features

No features have been removed from this release.

3.8 Version 5.0.17

Additional Features

The following features have been added to this release:

- Support for the SPC56EL70 (Leopard) and SPC56HK70 (Komodo) based on the MPC5643L and MPC5675K respectively. These have not been tested on real hardware.

Modified Features

The following features have been modified in this release:

- Corrects support for the SPC58NN84 (Bernina 6M) and SPC58NN84_JDP (Bernina 6M). Tested on real hardware.

Removed Features

No features have been removed from this release.

3.9 Version 5.0.16 (Preview Release)

Additional Features

The following features have been added to this release:

- Version 5.0.16 Preview.
- This preview is untested and strictly limited to evaluating the SPC58NN84 (Bernina) or SPC58NN84_JDP (Bernina) only.
- Support for 4.6.6.1 compiler in addition to previously supported compilers.
- Tested with the HighTec v4.6.6.1 compiler and only the MPC5746Mv2_JDP, SPC582B60 and SPC58NE84v2_JDP variants.
- Support for the SPC58NN84 (Bernina 6M) and SPC58NN84_JDP (Bernina 6M). These have not been tested on real hardware.
- Support for the cut 2 SPC58NE84v2 (Eiger 6M) and SPC58NE84v2_JDP (Eiger 6M). The SPC58NE84v2_JDP has been fully tested on real hardware.
- Support for the SPC582B60 (Chorus 1M). The SPC582B60 has been fully tested on real hardware.
- SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M). These have not been tested on real hardware.
- Support for the SPC582B50 (Chorus 512K), SPC58EC70 (Chorus 2M) and SPC58EC70_JDP (Chorus 2M) based upon the SPC582B60 (Chorus 1M), SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively.

Modified Features

The following features have been modified in this release:

- All SPC58xx84 (Eiger 6M) variants have been renamed to SPC58NE84 in order to differentiate from the SPC58NN84 (Bernina 6M).
- Variants MPC5673Fv2 and MPC5674Fv2 now utilize the instructions within the 'Volatile Context Save/Restore APU'.
- Updates to the cut 1 SPC58NE84 and SPC58NE84_JDP vector table.
- Syscall refactored and renamed to reduce the number of instructions.
- The example applications now support the MPC5746Mv2, MPC5777Mv2, SPC574K72v2, SPC582B60, SPC58EC80, SPC58NE84 and SPC58NE84v2 variants.

Removed Features

No features have been removed from this release.

3.10 Version 5.0.15

Additional Features

The following features have been added to this release:

- Version 5.0.15.
- Support for 4.6.6.0 compiler in addition to previously supported compilers.
- Support for the cut 2 MPC5746Gv2 (Calypso 3M) and cut 2 MPC5747Cv2 (Calypso 4M). This has not been tested on real hardware.
- Support for the MPC5746B (Calypso 3M) and MPC5746C (Calypso 3M). These have not been tested on real hardware.
- The target option 'Always call GetAbortStack' to always use Os_Cbk_GetAbortStack() to set up a safe area of memory to use as a stack when executing the ProtectionHook.
- The SPC582B60 (Chorus 1M) is shown as a selectable variant. However, this is a placeholder and must not be used.

Modified Features

The following features have been modified in this release:

- Updated the default implementation of Os_Cbk_GetAbortStack() so that no stack is used in both single and multicore applications.
- The code to support the 'enable stack repositioning' target option has been updated. The assembly language instructions generated now do not rely on values stored in the CPU general purpose registers to be preserved over the call to untrusted code.

Removed Features

The following features have been removed from this release:

- Support for the cut 1 MPC5673F, cut 1 MPC5674F and SPC582B.

3.11 Version 5.0.14

Additional Features

The following features have been added to this release:

- Supports Eiger chip, SPC58xx84 and SPC58xx84_JDP.
- Added the Os_IntChannel_x macro
- Target option: 'Cache CoreID'. e.g. for the Eiger, using '–target_option:Cache CoreID=PMGC0' will significantly improve performance, especially with untrusted code, because the Core ID is cached in the Performance Monitoring unit. This means that OS APIs can discover which core is running much faster. Other devices will be able to cache the Core ID in a SPRG register, but this is not possible on the Eiger. The Performance Monitoring unit cannot be used when this option is in effect.

Modified Features

The following features have been modified in this release:

- Standardized naming convention for 'Software Interrupt x' vectors.

Removed Features

No features have been removed from this release.

3.12 Version 5.0.13

Additional Features

The following features have been added to this release:

- Initial early access for Eiger chip, SPC58xx84/SPC58xx84_JDP ONLY. This version has undergone limited testing.
- Update for RTA-OS 5.4 compatibility
- Added experimental option: 'Cache CoreID'. For the Eiger using '–target_option:Cache CoreID=PMGC0' will significantly improve performance, especially with untrusted code, because the Core ID is cached in the Performance Monitoring unit. This means that OS APIs can discover which core is running much faster. Other devices will be able to cache the Core ID in a SPRG register, but this is not possible on the Eiger. The Performance Monitoring unit cannot be used when this option is in effect.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.13 Version 5.0.12

Additional Features

The following features have been added to this release:

- Addition of 'OS Locks disable Cat1' target option. This can be used to specify that all interrupts are disabled while internal OS spinlocks are held. This does not affect spinlocks accessed using the GetSpinlock or TryToGetSpinlock APIs.
- Support for compiler v4.6.5.0.
- Support for the MPC5748Gv2 (Calypso6M).
- Support for the MPC5748GCompatibility variant which shares the common interrupt vectors from the cut 1 and cut 2 MPC5748G devices.
- Initial support for the SPC584C (Chorus4M), SPC584B (Chorus2M) and SPC582B (Chorus1M). This is based solely upon the initial documentation and has not been tested on real hardware.
- Initial support for the MPC5746R (Rainier). This has not been tested on real hardware.

Modified Features

The following features have been modified in this release:

- Reduced library build time.
- Improvements to winIDEA ORTI and signalling to Profiler.
- Optimized buffer size and instructions used for both 32 and 64 bit implementations of Os_setjmp/Os_longjmp.

Removed Features

The following features have been removed from this release:

- Support for compiler v4.6.3.1.
- Support for the cut 1 MPC5748G.

3.14 Version 5.0.11

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- The software semaphore implementation now uses 32 bit decorated storage instructions instead of 8 bit versions.

Removed Features

No features have been removed from this release.

3.15 Version 5.0.10

Additional Features

The following features have been added to this release:

- Support for the cut 2 MPC5746Mv2 (McKinley) and JDP variant.
- Support for the MPC5777C (Cobra55) and MPC5645S (Spectrum).

Modified Features

The following features have been modified in this release:

- Support for using the 'Volatile Context Save/Restore APU' with Cat1 interrupts.
- The placement of Crosscore ISRs, Category 2 Os_wrapper and Spinlock functions into a CODE_FAST section (See Os_MemMap.h).

Removed Features

No features have been removed from this release.

3.16 Version 5.0.9

Additional Features

The following features have been added to this release:

- Initial support for 4.6.4.0 compiler
- For the cut 2 Matterhorn (MPC5777Mv2 and MPC5777Mv2_JDP), single writes to OS_INTC_CPR are used. (The cut 1 version needs double writes as an erratum workaround.)
- Support for the cut 2 MPC5744K/SPC574K72 and JDP variants.
- Support for the MPC5744P (Panther).
- The target option 'Emit stack usage' has been added to generate stack usage files using the -fstack-usage compiler option.
- The target option 'Generate Cat1 EOIR' has been added to generate code to write to the EOI register in Category 1 interrupts.

Modified Features

The following features have been modified in this release:

- Workaround added for software vectoring with MPC57xx devices. Priority inversion could occur with Category 2 ISRs.
- Modifications to cut 1 MPC5777M vector table.

Removed Features

No features have been removed from this release.

3.17 Version 5.0.8

Additional Features

The following features have been added to this release:

- Initial support for 4.6.3.1 compiler
- Additional vectors in MPC5673/4Fv2 vector table
- MPC5642A support
- SPC574K72, SPC574K72_JDP support
- MPC5748G support

Modified Features

The following features have been modified in this release:

- Adds support for MPC5777Mv2 and MPC5777Mv2_JDP.
- Disable interrupts on exit from CAT2 ISRs when using software-vectoring to reduce stack depth.

Removed Features

No features have been removed from this release.

3.18 Version 5.0.7

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Change software semaphore support to use a decorated storage instruction in the spinlock reset.

Removed Features

No features have been removed from this release.

3.19 Version 5.0.6

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Slight timing adjustment in software vectoring code for Cat2 ISRs, advised by Freescale. Without it interrupts raised via the SWT bit in a PSR might get missed.

Removed Features

No features have been removed from this release.

3.20 Version 5.0.5

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Removal of Freescale confirmed non-existing interrupt vectors 463, 475 and 539 from the MPC5777M/MPC5777M_JDP (Matterhorn) vector table.
- Fix for software vectoring configuration when repeatedly toggled using the respective option in the RTA-OS configuration GUI for a very specific use case.

Removed Features

No features have been removed from this release.

3.21 Version 5.0.4

Additional Features

The following features have been added to this release:

- Additional support for using a software semaphore instead of the SEMA4 hardware. The software semaphore option is only applicable to MPC57xx variants.
- Added initial support for using the ’Volatile Context Save/Restore APU’ when software vectoring is selected and using the MPC5777M or MPC5777M_JDP.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.22 Version 5.0.3

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- SRRx registers for the save/restore context are now also emitted for the Critical, Watchdog, MachineCheck and Debug IVOR interrupts.

Removed Features

No features have been removed from this release.

3.23 Version 5.0.2

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Fix to reinstate SRRx register code that was excluded from some IVOR interrupts.

Removed Features

No features have been removed from this release.

3.24 Version 5.0.1

Additional Features

The following features have been added to this release:

- Support for the MPC5674Fv2 (Silicon revision 2) to allow for the Performance Monitor Interrupt (IVOR 35) to be used. NOTE: The existing MPC5674F variant does not support this IVOR.

Modified Features

The following features have been modified in this release:

- Updated vector tables for the MPC57xx variants.

Removed Features

No features have been removed from this release.

3.25 Version 5.0.0

Additional Features

The following features have been added to this release:

- Support for HighTec compiler v4.6.2 only.

Modified Features

The following features have been modified in this release:

- Software vectoring: Optimized memory usage for Cat2 ISR decoding.
- Fix for 'Preserve SPE' target option to additionally work with 57xx variants by only preserving the SPEFSCR register.
- The example applications now support the MPC5726L, SPC572L64 and MPC5744K variants.

Removed Features

No features have been removed from this release.

3.26 Version 0.1.8

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Fixed an issue in Os_DisableInterrupts.h for the Os_DisableAllInterrupts/Os_EnableAllInterrupts macros that incorrectly listed category 1 interrupts.
- Fixed an issue with CPU vector generation for when raw interrupts are used.

Removed Features

The following features have been removed from this release:

- Support for the MPC5514.

3.27 Version 0.1.7

Additional Features

The following features have been added to this release:

- Support for MPC5744K_JDP (K2), MPC5726L (Lavaredo), MPC5726L_JDP (Lavaredo), SPC572L64 (Lavaredo) and SPC572L64_JDP (Lavaredo).
- Support for raw exception handlers selectable by a defined naming convention.
- The target option ’Block default interrupt’ has been added to set all unused interrupts to disabled with a default interrupt handler on the lowest priority.

Modified Features

The following features have been modified in this release:

- Addition of vector 533 SAR_ADC5 to the MPC5777M (Matterhorn) vector table.
- Fixed IVPR initialization in software vectoring mode for old-style target variants, e.g. SPC563M

Removed Features

The following features have been removed from this release:

- Support for HighTec compiler v4.6.1.0 due to incompatible options between it and the supported v4.6.2.0 HighTec compiler.
- Support for the MPC5516.

3.28 Version 0.1.6

Additional Features

The following features have been added to this release:

- Support for MPC5744K (K2).
- Support for the Performance Monitor Interrupt (IVOR 35) on z7 cores.
- The target options ’SDA ROM Threshold’ and ’SDA RAM Threshold’ have been added to support the use of the SDA.

Modified Features

The following features have been modified in this release:

- Corrected interrupt support for all MPC57xx devices bar the MPC5746M (McKinley) where no change was required.
- Added further compiler and linker options as requested, for example, -mfixed-sda.

Removed Features

No features have been removed from this release.

3.29 Version 0.1.5

Additional Features

The following features have been added to this release:

- HighTec compiler version 4.6.2.0 is supported.
- ORTI support for Cat1 ISRs in multicore configurations.
- Supports ’Enable stack repositioning’ option.
- The target option ’ORTI Stack Fill’ has been added to support debugger calculation of application stack usage using the ORTI details.
- The target option ’Support winIDEA Analyzer’ has been added to support the winIDEA debugger Analyzer features.
- Example code to demonstrate machine check exception handling.

Modified Features

The following features have been modified in this release:

- Fix to ’Enable untrusted stack check’ handling for Category 2 ISRs - could corrupt CR values.
- Category 2 interrupt handler supports interrupting of untrusted code in situations where the OS has not been configured to support untrusted TASKs or ISRs.
- Completion of target option to select software vectoring.
- Fix to provide the correct return from interrupt instruction on the IVOR interrupts.

Removed Features

No features have been removed from this release.

3.30 Version 0.1.4

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Updates software vectoring for user-supplied dispatcher and no vector table option

Removed Features

No features have been removed from this release.

3.31 Version 0.1.3

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Speed/size optimization for Category 2 ISRs with software vectoring.
- Fix for cross-core ISRs with hardware vectoring.
- Vector table for Matterhorn.

Removed Features

No features have been removed from this release.

3.32 Version 0.1.2

Additional Features

The following features have been added to this release:

- Added MPC5777M and MPC5777M_JDP variants (Matterhorn), based on the McKinley code. Untested on actual hardware currently.
- Adds target option to select software vectoring rather than hardware vectoring for dispatching INTC interrupts. This is a preliminary implementation. RTA-OS will supply the software dispatcher unless you configure your own CAT1 handler on IVOR4, in which case you can implement the sofware dispatcher yourself as a standard CAT1 ISR. For software vectoring, the Os_INTC_vectors table contains pointers to functions that take a uint32 argument that is the vector number, so you can use 'Os_INTC_vectors[vector](vector);' to perform the dispatching.

Modified Features

The following features have been modified in this release:

- This is an experimental release targeted at McKinley / Matterhorn only.

Removed Features

No features have been removed from this release.

3.33 Version 0.1.1

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Modified cross-core locking code slightly to avoid code starvation issues on a core trying to release a lock.

Removed Features

No features have been removed from this release.

3.34 Version 0.1.0

Additional Features

The following features have been added to this release:

- Added MPC5746M_JDP variant, which is the same as the MPC5746M but with the on-chip cores [0, 1, 2] mapping to AUTOSAR cores [1, 2, 0] (rather than [2, 1, 0])

Modified Features

The following features have been modified in this release:

- Each core gets its own Os_ISRWrapper as a preliminary to optimizations.

Removed Features

No features have been removed from this release.

3.35 Version 0.0.9

Additional Features

The following features have been added to this release:

- Testing done on a wider range of processors

Modified Features

The following features have been modified in this release:

- The cross-core interrupt selection option is changed so that only the first software interrupt is specified. The remaining cross-core interrupts will use consecutive vectors
- Drop the use of Os_isr_count on McKinley because there is a hardware workaround available

Removed Features

No features have been removed from this release.

3.36 Version 0.0.8

Additional Features

The following features have been added to this release:

- Experimental version. Implements double write to INTC

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.37 Version 0.0.7

Additional Features

The following features have been added to this release:

- Experimental version for detection of INTC issues on McKinley

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.38 Version 0.0.6

Additional Features

The following features have been added to this release:

- Experimental: nops in spinlock code to stop code starvation
- Experimental: Additional mbar/isync code
- -mno-regnames support

Modified Features

The following features have been modified in this release:

- Some MISRA work
- Fixes to systems with untrusted code (R4 getting clobbered)
- Fix for systems using just core 0 and 2 for OS

Removed Features

No features have been removed from this release.

3.39 Version 0.0.5

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Cope with spurious interrupts on McKinley - affected multicore operation only

Removed Features

No features have been removed from this release.

3.40 Version 0.0.4

Additional Features

The following features have been added to this release:

- Implement setjmp/longjmp internally
- Hello World Example links with reduced run-time library support

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.41 Version 0.0.3

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Change comment style in all .s files

Removed Features

No features have been removed from this release.

3.42 Version 0.0.2

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Support 64 interrupt priorities in RTAOSCFG
- Change comments in Os_Cat1.s

Removed Features

No features have been removed from this release.

3.43 Version 0.0.1

Additional Features

The following features have been added to this release:

- Initial early access for McKinley (MPC5746M). This release should only be used to evaluate the McKinley.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

4.1 Version 5.0.24

EHI 612096

Status: Fixed

Title: Incorrect time and stack measurements - software vectoring.

Description: The issue described in EHI 598673 was only fixed for hardware interrupt vectoring configurations. This version corrects the same issue in the software vectoring configurations.

EHI 613220

Status: Fixed

Title: Incorrect time and stack measurements - multicore.

Description: The issue described in EHI 598673 was only fixed for single-core configurations. This version corrects the same issue in the cross-core interrupt handler.

EHI 614899

Status: Fixed

Title: No SPE register saving when using software vectoring.

Description: The 'Preserve SPE' target option was not being considered when 'Use software vectoring' was TRUE. The SPE/EFPU2 related registers were not being saved and restored in the software vectoring handler.

EHI 614900

Status: Fixed

Title: Clarification of EOIR handling.

Description: The documentation has been improved to explain that Category 1 ISRs should not write EOIR when using software vectoring. EOIR should be written by Category 1 ISRs in hardware vectoring mode, but the 'Generate Cat1 EOIR' target option can be used to make this automatic.

EHI 620662

Status: Fixed

Title: Untrusted stack check functionality not working.

Description: In versions 5.0.17 to 5.0.23, the target option "Untrusted stack check" did not properly switch into untrusted mode to check the stack validity. The detection of an invalid stack might be delayed as a consequence.

4.2 Version 5.0.23

EHI 587529

Status: Fixed

Title: Incorrect boot core on the MPC5745R and MPC5746R.

Description: The boot core on the MPC5745R and MPC5746R was incorrectly implemented as chip core 0 but should be chip core 1 (Autosar core 0).

EHI 595061

Status: Fixed

Title: Corruption of SPE bit on some multicore core types

Description: For the variants MPC5676R, MPC5777C, MPC5643L/SPC56EL70, MPC5675K/SPC56HK70 and MPC5775K it was possible for an interrupt to pre-empt a cross core interrupt before it had preserved the state of the SPE bit for the code that it had pre-empted. This could result in the SPE bit getting switched off incorrectly. Applies to versions 5.0.21 and 5.0.22. Only applies if the 'Preserve SPE' target option is enabled.

EHI 598673

Status: Fixed

Title: Incorrect time and stack measurements

Description: It was possible for a Category 2 interrupt to pre-empt another Category 2 interrupt just before it had completed calculating time and stack values for the code that it had pre-empted. This could result in miscalculation of these values.

EHI 598674

Status: Fixed

Title: Failure to disable/restore MPU in interrupts when TrustedWithProtection OS Applications exist

Description: The MPU has to be enabled and disabled appropriately to support TrustedWithProtection on the PowerPC. Category 2. The code to do this was omitted in the Category 2 interrupt and cross-core interrupt handlers. This could result in the handler code wrongly running with the MPU enabled, which might result in incorrect memory traps. Alternatively it could result in the MPU being disabled when returning to pre-empted code.

4.3 Version 5.0.22 (Preview Release)

EHI 564982

Status: Fixed

Title: Incorrect value applied to the INTC_BCR register for hardware vectoring on the MPC5745R and MPC5746R.

Description: An incorrect value was written to the INTC_BCR register, resulting in hardware vectoring only applying to Autosar core 0. Only the MPC5745R and MPC5746R were affected.

EHI 577517

Status: Fixed

Title: Exception occurs in an untrusted OS application when "Enable stack repositioning" is enabled.

Description: The exception is caused by a write to an OS variable which can not be accessed once in untrusted mode. Only Tools 5.5.6+ and target v5.1.19+ are affected.

EHI 580178

Status: Fixed

Title: Use of xAllInterrupts APIs before StartOS() with "Cache CoreID" enabled.

Description: AUTOSAR states that the DisableAllInterrupts(), EnableAllInterrupts() and SuspendAllInterrupts(), ResumeAllInterrupts() APIs can be used before StartOS() is called. However with CoreID caching enabled the cached CoreID register had not yet been initialized.

EHI 584355

Status: Fixed

Title: Possible incorrect return address for ECC tasks that terminate.

Description: If an ECC task terminates by returning from the task body or calling TerminateTask() with lightweight termination active, the return address could be incorrect and cause a crash. ECC Tasks that only loop on WaitEvent and do not terminate are not affected.

4.4 Version 5.0.21

EHI 551514

Status: Fixed

Title: Changes to "Preserve SPE" target option functionality

Description: The OS now checks the MSR[SPE/SPV] bit to decide whether to preserve the appropriate registers. They are only preserved if it is set. This means that on devices such as the MPC5775K (where not all cores support SPE) it is now possible to control which cores use register preservation. It is normal for application code to initialize the SPE bit appropriately for each core before calling StartOS() and then not modify it afterwards. The OS will ensure that MSR[SPE] is preserved when interrupts or exceptions occur.

EHI 559949

Status: Fixed

Title: Attribute used for the vector table section address is no longer required

Description: The section attribute was required to support the 4.6.2.0 compiler but as that compiler is no longer supported the section attribute has been removed.

EHI 560828

Status: Fixed

Title: Incorrect MPC5775K vector table entries

Description: Interrupt vectors 746 to 749 were partially incorrect.

4.5 Version 5.0.20 (Preview Release)

EHI 558107

Status: Fixed

Title: Missing MPC5775K vector table entries

Description: Interrupt vectors 557 and 558 were missing from the vector table.

EHI 558262

Status: Fixed

Title: Crash caused by stack misalignment in ISRs when "Enable stack repositioning" was used with memory protection but the "Enable untrusted stack check" option was false.

Description: Applies only to RTA-OS 5.4.4 to 5.5.3. The ISR handler would not reset the stack after adjusting it to run the ISR. The workaround is to set "Enable untrusted stack check" option to true.

4.6 Version 5.0.16 (Preview Release)

EHI 498318

Status: Fixed
Title: Possible register corruption
Description: It is possible for register corruption to occur in the CallTrustedFunction API function when used to call untrusted functions (an RTA-OS extension to AUTOSAR). This will only occur if memory protection and stack realignment is enabled. This occurs on versions of the port before 5.0.15.

EHI 500990

Status: Fixed
Title: Incorrect MPC5744P vector table entry
Description: Interrupt vector 379 was considered a valid vector but is in fact reserved and not selectable. Interrupt vector 622 was duplicated, thus meaning vector 623 was missing.

EHI 501217

Status: Fixed
Title: Possible stack location swapped for Autosar cores 1 and 2 on 3 core JDP variants
Description: On the variants MPC5746M_JDP, MPC5746Mv2_JDP, MPC5777M_JDP, MPC5777Mv2_JDP and SPC58NE84_JDP it is possible that the generated example multicore start up code swaps the respective stack location for Autosar cores 1 and 2. The effect of this can lead to errors being reported on the wrong core and/or possible data corruption leading to a machine check exception. Port versions before 5.0.15 are affected by this issue.

EHI 528602

Status: Fixed
Title: Raw interrupts text
Description: Description of raw interrupt functionality added, whereby if an IVOR vector name is prefixed with 'b_' it allows the user to provide their own handler, as opposed to an RTA-OS generated handler.

4.7 Version 5.0.15

EHI 464449

Status: Fixed
Title: Preserve SPE target option text
Description: Improved clarity with regard to how this target option relates to the compiler and variant in use.

EHI 472743

Status: Fixed

Title: Os_Enable_ macros in Os_DisableInterrupts.h

Description: The macros generated in Os_DisableInterrupts.h for the MPC5643L, MPC5675K and SPC58xx84 parts were incorrect. They did not take account of the second INTC.

EHI 480159

Status: Fixed

Title: Backwards compatibility between Tools v5.4.3 and Tools v5.4.2

Description: ISR termination code generated by the target produced a compilation error in Os_Wrapper.c when using Tools v5.4.2 that was not present when using Tools v5.4.3.

EHI 485206

Status: Fixed

Title: Os_GetAbortStack buffer overflow

Description: On the K2 (all MPC5744K, all SPC574K72) and Calypso 4M (MPC5747Cv2) devices only, with the default implementation of Os_GetAbortStack, there will be an overflow if 'abortstack' is called on hardware core 2.

EHI 495715

Status: Fixed

Title: Example code for Os_Cbk_GetAbortStack might return NULL

Description: This occurs in configurations that use the Os_Cbk_SetMemoryAccess callback to update the memory protection settings for untrusted code, but where the stack value is not actually passed to the callback. i.e. Stack Monitoring is disabled AND target option 'Enable stack repositioning' is false a NULL value can be returned.

4.8 Version 5.0.14

EHI 448937

Status: Fixed

Title: Terminating ECC tasks with the Enable stack repositioning option

Description: If an interrupt occurred during the execution of the heavyweight version of TerminateTask for an ECC task, the setjmp/longjmp buffer used to return to the OS could become corrupted and cause unpredictable behavior. Note that ECC tasks do not normally terminate, so this should not be a common use-case.

EHI 450615

Status: Fixed

Title: Enable untrusted stack check

Description: The 'Enable untrusted stack check' in the interrupt handler was checking the preempted stack for both trusted and untrusted code. It should only have checked when it was preempting untrusted code, because the check switches briefly to untrusted mode. The stack might have been in a legal trusted area, but not a legal untrusted area. This could have caused a spurious protection trap, depending on the memory protection settings used.

4.9 Version 5.0.12

EHI 437256

Status: Fixed

Title: Possible overstated stack use.

Description: In configurations with stack monitoring enabled, a category 2 ISR pre-empting another ISR could cause the stack usage of the pre-empted task to appear to be higher than it should be. This is because some of the stack used by the pre-empted ISR was getting added to the task stack usage.

EHI 437404

Status: Fixed

Title: Os_InitializeVectorTable

Description: Os_InitializeVectorTable fails to disable all Cat 2 interrupts via the OS_INTC_CPRx register for a core ID greater than 1. Thus only 3 core variants were affected.

EHI 440614

Status: Fixed

Title: Early Task execution.

Description: On pre MPC57xx and MPC5777C variants that use the Os_isr_count variable to cope with a race condition in the INTC, configurations that enable stack or execution monitoring could run a task activated in a pre-empting category 2 ISR sooner than normal. The task should only run when the lowest priority ISR completes.

4.10 Version 5.0.10

EHI 403742

Status: Fixed

Title: Additional winIDEA ORTI instrumentation to TerminateTask.

Description:

4.11 Version 5.0.9

EHI 391988

Status: Fixed

Title: Addition of volatile to cast in Os_DisableInterrupts.h.

Description:

5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation	None.
Workaround	None.

5.2 PPCe200HighTec DLL

There are the following limitations for this tool:

Limitation	If a multicore variant does not enforce data coherency in hardware when the D-CACHE is enabled, then any data shared between cores has to use software mechanisms to flush/invalidate the cache. It is not currently clear how to do this efficiently in an AUTOSAR implementation.
Workaround	Do not enable D-CACHE.
Limitation	Remember that if you call Os_TimingFaultDetected from a Timing Protection interrupt, the interrupt handler will not exit normally so you will need perform EOIR directly in your handler.
Workaround	None.
Limitation	The MPC5748GCompatibility variant amalgamates the common interrupt vectors from the cut 1 and cut 2 silicon revisions and also facilitates the ability to run code on both silicon revisions. Note: the restriction on core 2 of cut 1 devices that hardware vectoring can not be used and that on cut 2 devices the clock dividers have changed.
Workaround	To fully utilize cut 2 silicon please use the MPC5748Gv2 variant.
Limitation	The MPC5644C, MPC5645C and MPC5646C are only supported as a single core variant, specifically the z4d core.
Workaround	None.

6 Contacting ETAS

6.1 Technical Support

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see Section 6.2.2).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline.uk@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- Your `.xml`, `.arxml` and `.rtaos` files
- The command line which caused the error
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The error message you received (if any)
- The file `Diagnostic.dmp` if it was generated

6.2 General Enquiries

6.2.1 ETAS Global Headquarters

ETAS GmbH

Borsigstrasse 24	Phone:	+49 711 3423-0
70469 Stuttgart	Fax:	+49 711 3423-2106
Germany	WWW:	www.etas.com

6.2.2 ETAS Local Sales & Support Offices

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

ETAS subsidiaries	www.etas.com/en/contact.php
ETAS technical support	www.etas.com/en/hotlines.php