RTA-OS PPCe200/WR

Release Note - Version 5.1.21 (11-06-2018)

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Safety Notice

This ETAS product fulfills standard quality management requirements. If requirements of specific safety standards (e.g. IEC 61508, ISO 26262) need to be fulfilled, these requirements must be explicitly defined and ordered by the customer. Before use of the product, customer must verify the compliance with specific safety standards.

Contents

1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS PPCe200/WR port plug-in that customizes the RTA-OS development tools for the Freescale/ST MPC5xxx/SPC5xx with the WindRiver (Diab) compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.1.21 of the RTA-OS PPCe200/WR plug-in.

1.2 Installation

The installation process is covered in detail in the *PPCe200WR Port Guide*.

2 Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.

3 Change History

3.1 Version 5.1.21

Additional Features

The following features have been added to this release:

- Support for the SPC582B54 (Chorus 768K) based upon the SPC582B60 (Chorus 1M).
- Support for the MPC5745B (Calypso 2M) based upon the MPC5746B (Calypso 3M).
- Support for the cut 2 MPC5745R (Rainier 3M) and cut 2 MPC5746R (Rainier 4M).
- Support for the S32R274 (RaceRunner Ultra) based upon the MPC5775K (RaceRunner).

Modified Features

The following features have been modified in this release:

- The example applications now support the MPC5745Rv2 (Rainier 3M) variant.

Removed Features

No features have been removed from this release.

3.2 Version 5.1.20 (Preview Release)

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Incorrect boot core on the MPC5745R and MPC5746R. See EHI 587406 in the ’Fixed EHI Calls’ section.
- The compiler option -Xdebug-local-cie is no longer a mandatory option for application code.

Removed Features

No features have been removed from this release.

3.3 Version 5.1.19

Additional Features

The following features have been added to this release:

- Initial support for the pre-production SPC58EG84 (Chorus 6M). The hardware we have has three cores but ST confirm the SPC58EG84 will only have two cores and it was this configuration that was tested. ST also inform us that the SPC58EG84 and SPC58NE84 are the same silicon. We note from our hardware that the JTAG ID is 0x11110041 and the contents of the MIDR1 register is 0x58884411, which differ from the SPC58NE84.
- Support for the MPC5604E based on data sheet only and not tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

The following features have been removed from this release:

- Support for the SPC584C.
- Support for the cut 1 MPC5744K and MPC5744K_JDP, SPC574K72 and SPC574K72_JDP.
- Support for the cut 1 MPC5746M and MPC5746M_JDP.
- Support for the cut 1 MPC5777M and MPC5777M_JDP.
- Support for the cut 1 SPC58NE84 and SPC58NE84_JDP.

3.4 Version 5.1.18

Additional Features

The following features have been added to this release:

- Support for the SPC570S40 based on data sheet only and not tested on real hardware.
- Support for the SPC574S60 based on data sheet only and not tested on real hardware.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.5 Version 5.1.17 (Preview Release)

Additional Features

The following features have been added to this release:

- Support for the Wind River 5.9.6.1 compiler.
- Support for the MPC5604E based on data sheet only and not tested on real hardware.
- Support for the RTA-OS 5.6 EnableInterruptSource and DisableInterruptSource APIs. The ClearPendingInterrupt API is not supported on the PowerPC because it is not feasible to do so.

Modified Features

The following features have been modified in this release:

- Corrected the core type and OS_INTC_x register addresses for the SPC584B (Chorus 2M).
- Clarification: When the 'Generate Cat1 EOIR' target option is disabled, it is permitted to modify the INTC_EOIR register (Or equivalent for Multicore) for category 1 interrupts only.

Removed Features

No features have been removed from this release.

3.6 Version 5.1.16

Additional Features

The following features have been added to this release:

- Support MPC5775K (RaceRunner), including testing on real hardware.
- Support MPC5745R (Rainier) based on data sheet only and not tested on real hardware.

10 Change History

- Support SPC58EG80 (Chorus 6M) based on data sheet only and not tested on real hardware.
- Support SPC584C74 (Chorus 4M) based on data sheet only and not tested on real hardware.
- Support for the SPC58EC74 (Chorus 3M) and SPC58EC74_JDP (Chorus 3M) based upon the SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively. These have not been tested on real hardware.
- Support for the SPC58NN84 (Bernina 6M) and SPC58NN84_JDP (Bernina 6M), including testing on real hardware.
- Supports trusted-with-protection OS Applications.
- The compile option -Xwhole-program-optim=0 has been added when building the RTA-OS library. Due to the huge number of potential RTA-OS codebases that can be generated, it is not possible to test the effects of whole-program-optimization on all of them. Therefore, we take the approach of excluding the RTA-OS library.

Modified Features

The following features have been modified in this release:

- All SPC58xx84 (Eiger 6M) variants have been renamed to SPC58NE84 in order to differentiate from the SPC58NN84 (Bernina 6M).
- Corrections to the cut 2 SPC58NE84v2 and SPC58NE84v2_JDP vector table.
- The 'Preserve SPE' target option is used to preserve SPE-related registers when preemption occurs. From this version onwards, the OS checks the MSR[SPE/SPV] bit to decide whether to preserve the appropriate registers. They are only preserved if it is set. This means that on devices such as the MPC5775K (where not all cores support SPE) it is now possible to control which cores use register preservation. It is normal for application code to initialize the SPE bit appropriately for each core before calling StartOS() and then not modify it afterwards. The OS will ensure that MSR[SPE] is preserved when interrupts or exceptions occur.
- Tuned SEMA4 handling code based on testing on the MPC5775K (RaceRunner).
- The example applications now support the MPC5775K (RaceRunner) variant.

Removed Features

No features have been removed from this release.

3.7 Version 5.1.15 (Preview Release)

Additional Features

The following features have been added to this release:

- This is a preview version that has preliminary support for OS Applications with TrustedApplicationWithProtection set. This behavior is available in RTA-OS from version 5.5.7.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.8 Version 5.1.14

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Tests complete for compiler version 5.9.4.7.
- The example applications now support the MPC5746Mv2, MPC5777Mv2, SPC574K72v2, SPC582B60, SPC58EC80, SPC58xx84 and SPC58xx84v2 variants.

Removed Features

No features have been removed from this release.

3.9 Version 5.1.13

Additional Features

The following features have been added to this release:

- Version 5.1.13 Preview.
- Support for the cut 2 SPC58xx84v2 (Eiger 6M) and SPC58xx84v2_JDP (Eiger 6M). The SPC58xx84v2 has been partially tested on real hardware.
- Support for the SPC582B50 (Chorus 512K), SPC58EC70 (Chorus 2M) and SPC58EC70_JDP (Chorus 2M) based upon the SPC582B60 (Chorus 1M), SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M) respectively.

Modified Features

The following features have been modified in this release:

- Updates to the cut 1 SPC58xx84 and SPC58xx84_JDP vector table.
- Variants MPC5673Fv2 and MPC5674Fv2 now utilize the instructions within the ’Volatile Context Save/Restore APU’.

Removed Features

No features have been removed from this release.

3.10 Version 5.1.12

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Tests complete for compiler version 5.9.4.7.

Removed Features

No features have been removed from this release.

3.11 Version 5.1.11

Additional Features

The following features have been added to this release:

- Support added for 5.8.0.0p5 and 5.8.0.0p6 compiler. Only tested on MPC5777C.
- 'Customer Option 1' added. Required RTA-OS version 5.4.4 or above.
- Support for the SPC582B60 (Chorus 1M), SPC58EC80 (Chorus 4M) and SPC58EC80_JDP (Chorus 4M). These have not been tested on real hardware.

Modified Features

The following features have been modified in this release:

- Syscall refactored and renamed to reduce the number of instructions.

Removed Features

The following features have been removed from this release:

- Support for the Wind River 5.9.4.4 compiler.
- Support for the cut 1 MPC5673F, cut 1 MPC5674F and SPC582B.

3.12 Version 5.1.10

Additional Features

The following features have been added to this release:

- Version 5.1.10 preview.
- Support for Wind River compiler 5.9.4.7 in addition to previously supported compilers.
- Compiler 5.9.4.7 is tested and only supported for the MPC5777Mv2 (Matterhorn).

Modified Features

No features have been modified in this release.

14 Change History

Removed Features

No features have been removed from this release.

3.13 Version 5.1.9

Additional Features

The following features have been added to this release:

- Support for Wind River compilers 5.9.4.0 and 5.9.4.4.
- Support for Wind River compiler 5.8.0.0 patch 5 on the MPC5676R (Cobra) only.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.14 Version 5.1.8

Additional Features

The following features have been added to this release:

- Version 5.1.8 preview.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.15 Version 5.1.7

Additional Features

The following features have been added to this release:

- Version 5.1.7 preview.
- Support for the Wind River 5.9.4.0 compiler in addition to the 5.9.4.4 compiler. NOTE: The Wind River 5.9.4.0 compiler is only supported and tested on the SPC563M variant.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.16 Version 5.1.6

Additional Features

The following features have been added to this release:

- Support for the MPC5746B (Calypso 3M) and MPC5746C (Calypso 3M). These have not been tested on real hardware.
- The target option 'Always call GetAbortStack' to always use Os_Cbk_GetAbortStack() to set up a safe area of memory to use as a stack when executing the ProtectionHook.

Modified Features

The following features have been modified in this release:

- Updated the default implementation of Os_Cbk_GetAbortStack() so that no stack is used in both single and multicore applications.
- The code to support the 'enable stack repositioning' target option has been updated. The assembly language instructions generated now do not rely on values stored in the CPU general purpose registers to be preserved over the call to untrusted code.
- Corrected multicore support for the MPC5746Gv2 and MPC5747Cv2.

Removed Features

No features have been removed from this release.

3.17 Version 5.1.5

Additional Features

The following features have been added to this release:

- Support for the Wind River 5.9.4.4 compiler. No earlier Wind River 5.9.4.x compilers are supported due to an inlining bug which affected the OS (see TC-DIAB12295).

16 Change History

- Support for the cut 2 MPC5746Gv2 (Calypso 3M) and cut 2 MPC5747Cv2 (Calypso 4M).
- Support for the MPC5748Gv2 (Calypso6M).
- Support for the MPC5748GCompatibility variant which shares the common interrupt vectors from the cut 1 and cut 2 MPC5748G devices.
- Supports Eiger chip, SPC58xx84 and SPC58xx84_JDP.
- A target option 'Use Short Enum' has been added that when set to 'true' will use the '-Xenum-is-short' compiler option. The default option is 'false', thus using the '-Xenum-is-int' compiler option.
- Explicitly added -Xpragma-section-first to the compiler options (This is the default compiler option).
- Added the Os_IntChannel_x macro
- Target option: 'Cache CoreID'. e.g. for the Eiger, using '–target_option:Cache CoreID=PMGC0' will significantly improve performance, especially with untrusted code, because the Core ID is cached in the Performance Monitoring unit. This means that OS APIs can discover which core is running much faster. Other devices will be able to cache the Core ID in a SPRG register, but this is not possible on the Eiger. The Performance Monitoring unit cannot be used when this option is in effect.
- Target option: 'OS Locks disable Cat1'. This can be used to specify that all interrupts are disabled while internal OS spinlocks are held. This does not affect spinlocks accessed using the GetSpinlock or TryToGetSpinlock APIs.

Modified Features

The following features have been modified in this release:

- Reduced library build time.
- Standardized naming convention for 'Software Interrupt x' vectors.

Removed Features

The following features have been removed from this release:

- Support for the cut 1 MPC5748G.
- Support for the SPC58EC.
- Support for the Wind River 5.9.3.0 and 5.9.3.2 compilers.

3.18 Version 5.1.4

Additional Features

The following features have been added to this release:

- Initial support for the SPC58EC (Chorus4M dual core), SPC584C (Chorus4M single core), SPC584B (Chorus2M) and SPC582B (Chorus1M). This is based solely upon the initial documentation and has not been tested on real hardware.
- Initial support for the MPC5746R (Rainier). This has not been tested on real hardware.

Modified Features

The following features have been modified in this release:

- Optimized buffer size when saving 64 bit registers and instructions used for both 32 and 64 bit implementations of Os_setjmp/Os_longjmp.
- Removal of isync in function Os_Flush_PTM because iSystem state that it isn't necessary.
- Prevent function Os_Flush_PTM being inlined.
- Category 1 ISR handling code moved to Os_text_vle section (was os_text_vle)

Removed Features

No features have been removed from this release.

3.19 Version 5.1.3

Additional Features

The following features have been added to this release:

- Support for the cut 2 MPC5746Mv2 (McKinley) and JDP variant.

Modified Features

The following features have been modified in this release:

- The software semaphore implementation now uses 32 bit decorated storage instructions instead of 8 bit versions.
- Improvements to winIDEA ORTI and signalling to Profiler.

18 Change History

Removed Features

No features have been removed from this release.

3.20 Version 5.1.2

Additional Features

The following features have been added to this release:

- Tested on 5.9.3.2 compiler. CAT1 ISR code may not compile correctly with version 5.9.3.2 if inlining optimization is enabled.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.21 Version 5.1.1

Additional Features

The following features have been added to this release:

- Support for the MPC5748G (Calypso), MPC5777C (Cobra55), MPC5645S (Spectrum) and MPC5744P (Panther)
- Support for the cut 2 MPC5744K/SPC574K72 and JDP variants.
- For the cut 2 Matterhorn (MPC5777Mv2 and MPC5777Mv2_JDP), single writes to OS_INTC_CPR are used. (The cut 1 version needs double writes as an erratum workaround.)
- The target option 'Generate Cat1 EOIR' has been added to emit code to write to the EOIR register in Category 1 ISRs.

Modified Features

The following features have been modified in this release:

- Adds support for MPC5777Mv2 and MPC5777Mv2_JDP.
- Updates to cut 1 MPC5777M vector table.
- Support for using the 'Volatile Context Save/Restore APU'. RTA-OS uses the APU for non-rfi based IVOR interrupts. Otherwise for all other Category 1 ISRs support is provided by the compiler.

- Workaround added for software vectoring with MPC57xx devices. Priority inversion could occur with Category 2 ISRs.
- The placement of Crosscore ISRs, Category 2 Os_wrapper and Spinlock functions into a CODE_FAST section (See Os_MemMap.h).

Removed Features

No features have been removed from this release.

3.22 Version 5.1.0

Additional Features

The following features have been added to this release:

- Added initial support for using the 'Volatile Context Save/Restore APU' when software vectoring is selected and using the MPC5777M or MPC5777M_JDP.

Modified Features

The following features have been modified in this release:

- Fix for MISRA compliance (correct handling of the macro semi-colon) in the generated Os_DisableInterrupts.h file.

Removed Features

No features have been removed from this release.

3.23 Version 5.0.90

Additional Features

The following features have been added to this release:

- Support for the Wind River 5.9.3.0 compiler.
- Support for the MPC5642A (Andorra) and SPC574K72/SPC574K72_JDP (K2) variants.
- Additional support for using a software semaphore instead of the SEMA4 hardware. The software semaphore option is only applicable to MPC57xx variants.

Modified Features

The following features have been modified in this release:

- Updates to the respective vector table for the MPC5777M (Matterhorn), MPC5673Fv2/MPC5674Fv2 (Mamba) variants.
- Slight timing adjustment in software vectoring code for Cat2 ISRs, advised by Freescale. Without it interrupts raised via the SWT bit in a PSR might get missed.
- Fix for software vectoring configuration when repeatedly toggled using the respective option in the RTA-OS configuration GUI for a very specific use case.

Removed Features

The following features have been removed from this release:

- Support for the Wind River 5.8.0.0 patch 5 compiler.

3.24 Version 5.0.22

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Re-introduce clear EE before raising IPL (removed in 5.0.21). Applies to non 57xx devices only.
- Faster setting untrusted mode

Removed Features

No features have been removed from this release.

3.25 Version 5.0.21

Additional Features

The following features have been added to this release:

- Support for the Performance Monitor Interrupt (IVOR 35) on z7 cores.
- Support for the MPC5674Fv2 (Silicon revision 2) to allow for the Performance Monitor Interrupt (IVOR 35) to be used. NOTE: The existing MPC5674F variant does not support this IVOR.
- Support for MPC5744K (K2), MPC5726L (Lavaredo) and SPC572L64 (Lavaredo).
- SRRx registers for the save/restore context are now also emitted for the Critical, Watchdog, MachineCheck and Debug IVOR interrupts.
- Double INTC_CPR writes are now enabled for all MPC57xx devices.
- Fix for 'Preserve SPE' target option to additionally work with 57xx variants by only preserving the SPEFSCR register.
- ORTI support for Cat1 ISRs in multicore configurations.
- Software vectoring: Optimized memory usage for Cat2 ISR decoding.

Modified Features

The following features have been modified in this release:

- Updated vector tables for the MPC57xx variants.
- The example applications now support the MPC5726L, SPC572L64 and MPC5744K variants.
- noadjust has been added to the stack get and set functions.
- Support for compiler version 5.8.0.0 up to and including patch 5 only. Patch 6 generates erroneous warnings when C condition expressions use enums (see WIND00400165).

Removed Features

No features have been removed from this release.

3.26 Version 5.0.20

Additional Features

The following features have been added to this release:

- Version 5.0.20 Release

Modified Features

The following features have been modified in this release:

- Removes dependency on asm.h

Removed Features

No features have been removed from this release.

3.27 Version 5.0.18

Additional Features

The following features have been added to this release:

- Supports ’Enable stack repositioning’ option
- Enhanced support for winIDEA debugger and ORTI stack monitoring

Modified Features

The following features have been modified in this release:

- Fix to ’Enable untrusted stack check’ handling for Category 2 ISRs - could corrupt CR values
- Tidy-up in the MachineCheckException sample

Removed Features

No features have been removed from this release.

3.28 Version 5.0.3

Additional Features

The following features have been added to this release:

- Added MPC5777M and MPC5777M_JDP variants (Matterhorn), based on the McKinley code.
- Adds target option to select software vectoring rather than hardware vectoring for dispatching INTC interrupts. RTA-OS will supply the software dispatcher unless you configure your own CAT1 handler on IVOR4, in which case you can implement the software dispatcher yourself as a standard CAT1 ISR. For software vectoring, the Os_INTC_vectors table contains pointers to functions that take a uint32 argument that is the vector number, so you can use 'Os_INTC_vectors[vector](vector);' to perform the dispatching.
- Standardizes code across other PPC compiler ports

Modified Features

The following features have been modified in this release:

- Updates software vectoring for user-supplied dispatcher and no vector table option
- Category 2 interrupt handler supports interrupting of untrusted code in situations where the OS has not been configured to support untrusted TASKs or ISRs.
- Modified cross-core locking code slightly to avoid code starvation issues on a core trying to release a lock.

Removed Features

No features have been removed from this release.

3.29 Version 5.0.2

Additional Features

The following features have been added to this release:

- The target option 'SDA ROM Threshold' has been added to support setting the threshold for the -Xsmall-const compilation option used when compiling the RTA-OS library.

- The target option ’ORTI Stack Fill’ has been added to support debugger calculation of application stack usage using the ORTI details.
- The target option ’Support winIDEA Analyzer’ has been added to support the winIDEA debugger Analyzer features.
- Example code to demonstrate machine check exception handling

Modified Features

The following features have been modified in this release:

- The target option ’SDA Threshold’ has been modified to ’SDA RAM Threshold’ to clarify that this option only affects the -Xsmall-data compiler option.
- The ORTI support for the winIDEA and Lauterbach debuggers now tracks Category 1 Interrupts.
- Adjustments to INTC priority handling to remove priority inversion on certain parts. Necessary on multicore parts.

Removed Features

The following features have been removed from this release:

- Support for McKinley (MPC5746M). This part will be supported in the next release.

3.30 Version 5.0.1

Additional Features

The following features have been added to this release:

- Initial early access for McKinley (MPC5746M). This release should only be used to evaluate the McKinley.
- Deprecation warning: This is the last version that supports compiling the OS with Non-VLE code. Future versions will be VLE-only. Application code does not have to be VLE.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.31 Version 5.0.0

Additional Features

The following features have been added to this release:

- Version 5.0.0 Release

Modified Features

The following features have been modified in this release:

- The minimum stack granularity has been adjusted to 8 bytes.
- WaitEvent has been optimized to improve speed.
- The setjmp/longjmp functions have been optimized for size and speed.

Removed Features

No features have been removed from this release.

3.32 Version 4.99.0

Additional Features

The following features have been added to this release:

- Version 4.99.0 preview
- The target option 'Preserve SPE', when TRUE, causes the OS to preserve the full 64-bit versions of the registers r0, r3 to r12 plus the two SPE related registers ACC and SPEFSCR across TASK and Category 2 interrupts preemptions. When FALSE (the default), only the normal 32-bit registers are preserved, saving time and memory.
- The target option 'Avoid run-time library' can be used to ensure that internal versions of methods such as setjmp/longjmp and memset are used rather than the versions in the compiler toolchain library. This is the default behavior now. You can set this to FALSE to use the toolchain supplied versions. NOTE: Because the compiler recognizes setjmp and longjmp as 'special', it has been necessary to use these names rather than prefixing them with Os_ as we would normally do.

Modified Features

The following features have been modified in this release:

- Actions have been taken to ensure that re-ordering of inline assembly code cannot occur in the generated library.
- The Port Guide documents the target-specific APIs and macros.
- The sample applications have been checked and cleaned up.

Removed Features

No features have been removed from this release.

3.33 Version 2.0.10

Additional Features

The following features have been added to this release:

- This final release synchronizes with RTA-OS 5.0.0.
- StartCore now calls Os_Cbk_StartCore() to implement releasing non-master cores. Library slightly restructured to support demand-link replacement of multicore elements.

Modified Features

The following features have been modified in this release:

- Completes RTA-TRACE support for Multicore.
- MSR[EE] is set initially during StartOS to be sure interrupts can preempt autostarted tasks.
- Clock rates for sample applications corrected on Cobra part.
- Enhanced debug support for Leopard memory areas.
- Example linker files cleaned up.

Removed Features

No features have been removed from this release.

3.34 Version 2.0.8

Additional Features

The following features have been added to this release:

- This release synchronizes with RTA-OS 4.94.0.
- Multicore: The SEMA4 channel used for Spinlocks can be configured.
- Multicore: The software interrupts used for cross-core communication can be configured.
- Multicore: Support for Leopard in addition to Cobra.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.35 Version 2.0.7

Additional Features

The following features have been added to this release:

- This release synchronizes with RTA-OS 4.93.0 and is functionally complete regarding the AUTOSAR requirements.

Modified Features

The following features have been modified in this release:

- Code generated as assembler files (e.g. vectors) is placed in .os_text or .os_vle_text sections.

Removed Features

No features have been removed from this release.

3.36 Version 2.0.6

Additional Features

The following features have been added to this release:

- MultiCore ECC support

28 Change History

Modified Features

The following features have been modified in this release:

- This release synchronizes with RTA-OS 4.92.3

Removed Features

No features have been removed from this release.

3.37 Version 2.0.5

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- This release synchronizes with RTA-OS 4.92.2
- Lint/MISRA tweaks (PC-lint version 9)
- Access to core ID is provided for untrusted code and code before StartOS (before StartOS, code must be trusted)
- Reduce compiler optimization on selected files (was eliminating asm statements)
- Skip checking for core ID in single core configurations
- Avoid potential for undue nesting in cross core ISRs

Removed Features

No features have been removed from this release.

3.38 Version 2.0.4

Additional Features

No features have been added to this release.

Modified Features

The following features have been modified in this release:

- Support for both RAM and Flash based applications - enabling cache, selecting round-robin and enabling cache coherency. MAS values preliminary.
- Category 2 interrupt handlers have different entry points for different cores. Each one uses a different Os_Isr_count variable.
- This release must be used with RTA-OS version 4.92.1

Removed Features

No features have been removed from this release.

3.39 Version 2.0.3

Additional Features

The following features have been added to this release:

- Initial preliminary multi-core support for the MPC5676R. Requires RTA-OS5 kernel support.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.40 Version 2.0.2

Additional Features

The following features have been added to this release:

- Completed release

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

30 Change History

3.41 Version 2.0.0

Additional Features

The following features have been added to this release:

- Initial Beta release.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

4.1 Version 5.1.20 (Preview Release)

EHI 587406

Status:	Fixed
Title:	Incorrect boot core on the MPC5745R and MPC5746R.
Description:	The boot core on the MPC5745R and MPC5746R was incorrectly implemented as chip core 0 but should be chip core 1 (Autosar core 0).

4.2 Version 5.1.19

EHI 583930

Status:	Fixed
Title:	Incorrect SPC570S40 vector table entries
Description:	Interrupt vectors 690 to 701 were missing.

EHI 584354

Status:	Fixed
Title:	Possible incorrect return address for ECC tasks that terminate.
Description:	If an ECC task terminates by returning from the task body or calling TerminateTask() with lightweight termination active, the return address could be incorrect and cause a crash. ECC Tasks that only loop on WaitEvent and do not terminate are not affected.

4.3 Version 5.1.17 (Preview Release)

EHI 577516

Status:	Fixed
Title:	Exception occurs in an untrusted OS application when "Enable stack repositioning" is enabled.
Description:	The exception is caused by a write to an OS variable which can not be accessed once in untrusted mode. Only Tools 5.5.6+ and target v5.1.15+ are affected.

EHI 580177

Status: Fixed

Title: Use of xAllInterrupts APIs before StartOS() with "Cache CoreID" enabled.

Description: AUTOSAR states that the DisableAllInterrupts(), EnableAllInterrupts() and SuspendAllInterrupts(), ResumeAllInterrupts() APIs can be used before StartOS() is called. However with CoreID caching enabled the cached CoreID register had not yet been initialized.

4.4 Version 5.1.16

EHI 528603

Status: Fixed

Title: Raw interrupts text

Description: The Port Guide now describes the 'raw interrupt' feature. If a Category 1 IVOR ISR name starts with 'b_' then the interrupt branches directly to the handler and omits any RTA-OS support code.

EHI 552210

Status: Fixed

Title: Crash caused by stack misalignment in ISRs when "Enable stack repositioning" was used with memory protection but the "Enable untrusted stack check" option was false.

Description: Applies only to RTA-OS 5.4.4 to 5.5.3. The ISR handler would not reset the stack after adjusting it to run the ISR. The workaround is to set "Enable untrusted stack check" option to true.

EHI 564965

Status: Fixed

Title: Incorrect value applied to the INTC_BCR register for hardware vectoring on the MPC5745R and MPC5746R.

Description: An incorrect value was written to the INTC_BCR register, resulting in hardware vectoring only applying to Autosar core 0. Only the MPC5745R and MPC5746R were affected.

4.5 Version 5.1.12

EHI 500984

Status: Fixed

Title: Incorrect MPC5744P vector table entries

Description: Interrupt vector 379 was considered a valid vector but is in fact reserved and not selectable. Interrupt vector 622 was duplicated, and vector 623 was missing.

EHI 501214

Status: Fixed

Title: Possible register corruption

Description: It is possible for register corruption to occur in the CallTrustedFunction API function when it is used to call untrusted functions (an RTA-OS extension to AUTOSAR) and the code in the untrusted function corrupts registers. This will only occur if memory protection and stack realignment is enabled. This occurs on versions of the port before 5.1.6.

EHI 501216

Status: Fixed

Title: Possible stack location swapped for Autosar cores 1 and 2 on 3 core JDP variants

Description: On the variants MPC5746M_JDP, MPC5746Mv2_JDP, MPC5777M_JDP, MPC5777Mv2_JDP and SPC58xx84_JDP it is possible that the generated example multicore start up code swaps the respective stack location for Autosar cores 1 and 2. The effect of this can lead to errors being reported on the wrong core and/or possible data corruption leading to a machine check exception. Port versions before 5.1.8 are affected by this issue.

4.6 Version 5.1.11

EHI 495716

Status: Fixed

Title: Example code for Os_Cbk_GetAbortStack might return NULL.

Description: This occurs in configurations that use the Os_Cbk_SetMemoryAccess callback to update the memory protection settings for untrusted code, but where the stack value is not actually passed to the callback. i.e. Stack Monitoring is disabled AND target option 'Enable stack repositioning' is false. The supplied Os_Cbk_GetAbortStack implementation is a default that can be overridden by a customer.

4.7 Version 5.1.10

EHI 485205

Status: Fixed

Title: Os_GetAbortStack buffer overflow

Description: On the K2 (all MPC5744K, all SPC574K72) and Calypso 4M (MPC5747Cv2) devices only, with the default implementation of Os_GetAbortStack, there will be an overflow if 'abortstack' is called on hardware core 2.

4.8 Version 5.1.8

EHI 472957

Status: Fixed

Title: Os_Enable_ macros in Os_DisableInterrupts.h

Description: The macros generated in Os_DisableInterrupts.h for the MPC5643L, MPC5675K and SPC58xx84 parts were incorrect. They did not take account of the second INTC.

EHI 480158

Status: Fixed

Title: Backwards compatibility between Tools v5.4.3 and Tools v5.4.2

Description: ISR termination code generated by the target produced a compilation error in Os_Wrapper.c when using Tools v5.4.2 that was not present when using Tools v5.4.3.

4.9 Version 5.1.6

EHI 464449

Status: Fixed

Title: Preserve SPE target option text

Description: Improved clarity with regard to how this target option relates to the compiler and variant in use.

4.10 Version 5.1.5

EHI 433883

Status: Fixed

Title: -Xnested-interrupts

Description: The port guide is updated to show that the compiler option -Xnested-interrupts is also needed for application code (to support the CAT1_ISR macro)

EHI 437256

Status: Fixed

Title: Possible overstated stack use.

Description: In configurations with stack monitoring enabled, a category 2 ISR pre-empting another ISR could cause the stack usage of the pre-empted task to appear to be higher than it should be. This is because some of the stack used by the pre-empted ISR was getting added to the task stack usage.

EHI 437404

Status: Fixed

Title: Os_InitializeVectorTable

Description: Os_InitializeVectorTable fails to disable all Cat 2 interrupts via the OS_INTC_CPRx register for a core ID greater than 1. Thus only 3 core variants were affected.

EHI 440614

Status: Fixed

Title: Early Task execution.

Description: On pre MPC57xx and MPC5777C variants that use the Os_isr_count variable to cope with a race condition in the INTC, configurations that enable stack or execution monitoring could run a task activated in a pre-empting category 2 ISR sooner than normal. The task should only run when the lowest priority ISR completes.

EHI 448937

Status: Fixed

Title: Terminating ECC tasks with the Enable stack repositioning option

Description: If an interrupt occurred during the execution of the heavyweight version of TerminateTask for an ECC task, the setjmp/longjmp buffer used to return to the OS could become corrupted and cause unpredictable behavior. Note that ECC tasks do not normally terminate, so this should not be a common use-case.

EHI 450615

Status: Fixed

Title: Enable untrusted stack check

Description: The ’Enable untrusted stack check’ in the interrupt handler was checking the preempted stack for both trusted and untrusted code. It should only have checked when it was preempting untrusted code, because the check switches briefly to untrusted mode. The stack might have been in a legal trusted area, but not a legal untrusted area. This could have caused a spurious protection trap, depending on the memory protection settings used.

4.11 Version 5.1.1

EHI 403742

Status: Fixed

Title: Additional winIDEA ORTI instrumentation to TerminateTask.

Description:

5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation	None.
Workaround	None.

5.2 PPCe200WR DLL

There are the following limitations for this tool:

Limitation	The WR linker is able to detect branch instructions where the branch offset is out of the range for the op-code. It can insert 'branch islands' into the executable file that use registers R12 and CTR to calculate the absolute address before jumping to the address in CTR. Because this happens in the linker, no evidence is seen for this in the source code, listings or object files so it is very hard to detect when this occurs. The only place that could possibly affect OS code is where branches in Os_Vectors.s have offsets to trap or interrupt handlers that are very far away from them. These branches occur as the very first part of interrupt handlers, before R12 and CTR have been saved. This can result in corruption of R12 and CTR in interrupted code.
Workaround	Ensure that the interrupt handler code is located within 32M of the Os_Vectors code. Ideally specify that the linker may not insert branch-islands, so you would see a link failure rather than having the code silently changed during linking.

Limitation	RTA-OS uses the __interrupt__ modifier in the CAT1_ISR macro. This means that compiler determines which registers to preserve for such Category 1 interrupts. The choice of registers is not affected by the value of the 'Preserve SPE Registers' target option.
Workaround	Check that the compiler preserves the appropriate registers in your CAT1_ISR interrupts.

Limitation If a multicore variant does not enforce data coherency in hardware when the D-CACHE is enabled, then any data shared between cores has to use software mechanisms to flush/invalidate the cache. It is not currently clear how to do this efficiently in an AUTOSAR implementation.

Workaround Do not enable D-CACHE.

Limitation Remember that if you call Os_TimingFaultDetected from a Timing Protection interrupt, the interrupt handler will not exit normally so you will need perform EOIR directly in your handler.

Workaround None.

Limitation ETAS is currently working with Freescale regarding an issue with the Machine Check Interrupt, specifically the MCSRR0 register on the MPC5777C variant. It is hoped that the issue will be resolved by the next release of the port.

Workaround Freescale have now confirmed that the MCSRR0 register will not hold the instruction that actually caused a Machine Check Exception but instead an instruction from a few cycles later. If the instruction cache(s) are disabled the MCSRR0 register will hold the instruction that actually caused the Machine Check Exception.

Limitation The MPC5748GCompatibility variant amalgamates the common interrupt vectors from the cut 1 and cut 2 silicon revisions and also facilitates the ability to run code on both silicon revisions. Note: the restriction on core 2 of cut 1 devices that hardware vectoring can not be used and that on cut 2 devices the clock dividers have changed.

Workaround To fully utilize cut 2 silicon please use the MPC5748Gv2 variant.

Limitation Decorated storage instructions where a CPU accesses a slave on the other crossbar. There is an issue confirmed by ST (PS1448) which affects the correct operation of decorated storage instructions on a cut 1 Eiger/Chorus. The issue is that the locking signal between crossbars is not present and therefore the read, modify, write sequence is no longer atomic.

Workaround It is advised to use the SEMA4 unit instead.

Limitation The MPC5644C, MPC5645C and MPC5646C are only supported as a single core variant, specifically the z4d core.

Workaround None.

Limitation The RTA-OS 5.6 ClearPendingInterrupt API is not supported on the PowerPC because it is not feasible to do so. The API will return E_OS_ID for all ISRs.

Workaround None.

6 Contacting ETAS

6.1 Technical Support

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see Section 6.2.2).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline.uk@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- Your `.xml`, `.arxml`, `.rtaos` and/or `.stc` files
- The command line which caused the error
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The error message you received (if any)
- The file `Diagnostic.dmp` if it was generated

6.2 General Enquiries

6.2.1 ETAS Global Headquarters

ETAS GmbH

Borsigstrasse 24	Phone:	+49 711 3423-0
70469 Stuttgart	Fax:	+49 711 3423-2106
Germany	WWW:	www.etas.com

6.2.2 ETAS Local Sales & Support Offices

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

ETAS subsidiaries	www.etas.com/en/contact.php
ETAS technical support	www.etas.com/en/hotlines.php