

RTA-OS RH850x2/GHS

Release Note - Version 5.0.3 (18-06-2019)



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1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS RH850x2/GHS port plug-in that customizes the RTA-OS development tools for the Renesas RH850x2 with the GREENHILLS compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.0.3 of the RTA-OS RH850x2/GHS plug-in.

1.2 Installation

The installation process is covered in detail in the RH850x2GHS Port Guide.



2 Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.



3 Change History

3.1 Version 5.0.3

Additional Features

The following features have been added to this release:

- Note that this target port will only work with RTA-OS Tools v5.5.6 or later.
- The target option Core Specific Wrappers has been added to allow you to locate the outer and mid interrupt wrappers for Table Reference mode EIINT ISRs in core specific sections. The wrappers for an ISR assigned to core x will be located in the section Os_primitivesx. E.g. The wrappers for an ISR assigned to core 0 will be located in the section Os_primitives0 and the wrappers for an ISR assigned to core 2 will be located in the section Os primitives2.

Modified Features

The following features have been modified in this release:

- The exemplar linker scripts now contain sections for core-local data.
- The shim functions used for category 2 ISRs (Os_shim_XXX) are now placed in Os_MemMap.h controlled sections OS_START_SEC_COREx_CODE_LIB where x is the core to which the ISRs are assigned. E.g. the shim for an ISR that is assigned to core 0 will be placed in the Os_MemMap.h controlled section OS_START_SEC_CORE0_CODE_LIB and the shim for an ISR that is assigned to core 2 will be placed in the section OS_START_SEC_CORE2_CODE_LIB.

Removed Features

No features have been removed from this release.

3.2 Version 5.0.2 (Preview Release)

Additional Features

The following features have been added to this release:

- Enhanced isolation support. Please see the document RTA-OS RH850x2GHS Enhanced Isolation.pdf.
- Added vector labels for the U2A.
- Now supports the U2A16 developed from datasheet, not tested on EVB.
- Now supports the U2A8 developed from datasheet, not tested on EVB.
- The function Os_Get_CoreID() has been added to the RTA-OS library to support reading the core identifier.



Modified Features

The following features have been modified in this release:

- When an ISR is attached to the vector for an INTC1 interrupt channel, Os_InitializeVectorTable() will only enable the interrupt channel on the core to which the ISR is assigned in the configuration.
- The Os_DisableAllConfiguredInterrupts and Os_EnableAllConfiguredInterrupts macros have been replaced with Os_DisableAllConfiguredInterrupts_Corex and Os_EnableAllConfiguredInterrupts_Corex that only disable and enabled interrupt channels whose ISRs have been assigned to core x in the configuration. x is the numeric value found in a core's PEID register. E.g. Os_DisableAllConfiguredInterrupts_Core0 disables interrupt channels on the core whose PEID register contains the value 0 and Os_DisableAllConfiguredInterrupts_Core1 disables interrupt channels on the core whose PEID register contains the value 1.
- By default the core ID is not now cached in the CTPC register. Core ID caching can now be enabled using a target option.
- The RTA-OS generated vector table does not include the reset vector and is now aligned to 16 bytes so that a reset vector can be placed immediately before it. Please see the samples applications for an example.
- The vector labels for the E2GM, E2L and E2M have been updated.
- Changed the inline function in Os.h (e.g. OS_STCW and OS_CLR1) so that they do not results in compiler errors.
- All CPU vectors must now be IPL 17. ElINT vectors must have IPLs 1-16.
- Os_setjmp/Os_longjmp now saves r1 and r30 for alignment with GHS library versions of setjmp/longjmp.

Removed Features

No features have been removed from this release.

3.3 Version 5.0.1 (Preview Release)

Additional Features

The following features have been added to this release:

- Interim preview release
- Support for the U2A (Vector table labels to be added).
- New API Os CacheCoreID() to store the core ID in CTPC.
- In multi-core configurations Os InitializeVectorTable() now calls Os CacheCoreID().



Modified Features

The following features have been modified in this release:

- Cross-core interrupt handling has been re-written to use a single IPIR channel. The first free IPIR channel is always used.
- Changed the behavior when the ProtectionHook is called so that the PSW.ID and/or PSW.NP bits are not cleared. Please see the section 'Recovering from CPU Exceptions/Interrupts that call the ProtectionHook' in the port guide.
- Updated the behavior of the Os_ConfigInterrupts.h macros to use the Green Hills intrinsic functions __CLR1() and __SET1().
- Updated the behavior of the Interrupt Source API to use the Green Hills intrinsic functions __CLR1() and __SET1().

Removed Features

The following features have been removed from this release:

Removed the 'Default interrupt low priority' target option.

3.4 Version 5.0.0

Additional Features

The following features have been added to this release:

First release

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.



4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

4.1 Version 5.0.2 (Preview Release)

EHI 599983

Status: Fixed

Title: TerminateApplication.c Compilation Failure

Description: With RTA-OS tools prior to 5.6.3, under some circum-

stances when enhanced isolation and application terminate were enabled, there would be an error compiling TerminateApplication.c due to "calling_application" not being

defined. This has been fixed.



5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation None. **Workaround** None.

5.2 RH850x2GHS DLL

There are the following limitations for this tool:

Limitation At the time of writing the Lauterbach debugger used was not able

to successfully program flash on the U2A. Therefore the example

applications do not include .cmm scripts for running out of flash.

Workaround None.



6 Contacting ETAS

6.1 Technical Support

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see Section 6.2.2).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline.uk@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- Your .xml, .arxml, .rtaos and/or .stc files
- The command line which caused the error
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The error message you received (if any)
- The file Diagnostic.dmp if it was generated

6.2 General Enquiries

6.2.2

6.2.1 ETAS Global Headquarters

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