

RTA-OS RH850x2/WR

Release Note - Version 5.0.3 (15-01-2019)



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Safety Notice

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1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS RH850x2/WR port plug-in that customizes the RTA-OS development tools for the Renesas RH850x2 with the WIN-DRIVER_DIAB compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 5.0.3 of the RTA-OS RH850x2/WR plug-in.

1.2 Installation

The installation process is covered in detail in the RH850x2WR Port Guide.



2 Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.



3 Change History

3.1 Version 5.0.3

Additional Features

The following features have been added to this release:

- In multicore configurations Os InitializeVectorTable() now calls Os CacheCoreID().
- The Os CacheCorelD() function has been moved to its own file in the library.

Modified Features

The following features have been modified in this release:

• The sample applications now use the TPTM module to implement the stopwatch. This allows a stopwatch tick to be the same time period as a processor cycle.

Removed Features

No features have been removed from this release.

3.2 Version 5.0.2 (Preview Release)

Additional Features

The following features have been added to this release:

- Pre-release software, not fully tested and subject to change in future releases. Must not be used in production software.
- Now supports E2GM tested on E2GM EVB.
- Now supports E2GUH tested on E2GUH EVB.
- Now supports E2GH developed from datasheet, not tested on EVB.
- Now supports E2H developed from datasheet, not tested on EVB.
- Now supports E2L developed from datasheet, not tested on EVB.
- Now supports E2M developed from datasheet, not tested on EVB.
- Now supports E2UH developed from datasheet, not tested on EVB.
- New API Os CacheCoreID() to store the core ID in CTPC.
- Trusted-with-protection fixes for ISRs.
- Bug fix for entry to ISRs when stack and/or time monitoring is enabled. When a
 category 2 interrupt occurs and stack/time monitoring is enabled the IPL is now
 raised to the IPL of the highest category 2 ISR until the stack/time monitoring logic
 has been performed.



- StartOS() now checks that the process is in the correct state to run the OS. Please see the port guide for details.
- The port guide now contains documentation for Os InitializeVectorTable().

Modified Features

The following features have been modified in this release:

- Cross-core interrupt handling has been re-written to use a single IPIR channel. The
 first free IPIR channel is always used so the 'CrossCoreN IPIR' target options are no
 longer needed or supported.
- Extended ORTI support to include Category 1 interrupts.
- Updated exemplar debugger scripts to prepare memory for ORTI stack tracing and added support to the sample applications to support ORTI stack tracing.
- Updated spin-lock code to improve fairness when locks are used between core clusters.
- Fixed a bug when the 'Enable untrusted stack check' target option was true where the wrong core's temporary storage was used for cores numbers > 1.
- Changed the behavior when the ProtectionHook is called so that the PSW.ID and/or PSW.NP bits are not cleared. Please see the section 'Recovering from CPU Exceptions/Interrupts that call the ProtectionHook' in the port guide.
- Fixed a bug where the PSW was not restored correctly if an FE trap/interrupt was pre-empted by another FE trap/interrupt.
- Fixed a bug where the default Os_GetAbortStack() function was not being correctly generated for multicore builds.
- Moved the prototypes for _ldlw() and _stcw() so that they do not appear in Os.h to avoid conflicts with necasm.h.
- Moved several declarations out of Os ConfigInterrupts.h into Os.h.
- Revised and corrected the names of interrupt vectors.

Removed Features

The following features have been removed from this release:

• Removed the 'Default interrupt low priority' target option'.



3.3 Version 5.0.1 (Preview Release)

Additional Features

The following features have been added to this release:

- Pre-release software, not fully tested and subject to change in future releases. Must not be used in production software.
- Adds untested support for the FCC2 family of chips, including the E2GUH, E2UH, E2GH and E2H.
- Support for the Wind River 5.9.6.4 compiler in addition to 5.9.6.2

Modified Features

The following features have been modified in this release:

- Cross-core interrupt handlers now have per-core implementations, which their performance
- Category 2 ISR handlers now have per-core implementations, which improves their performance

Removed Features

No features have been removed from this release.

3.4 Version 5.0.0

Additional Features

The following features have been added to this release:

First release

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.



4 Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls have been fixed in this release.



5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation None. **Workaround** None.

5.2 RH850x2WR DLL

There are the following limitations for this tool:

Limitation

This target port uses the same vector tables on all cores and Os_InitializeVectorTable() enables configured INTC1 interrupts on all cores - not just the core to which they are attached in the project configuration. This means that the ISR for a CPU interrupt or an INTC1 interrupt can be invoked on any core (assuming it is triggered by a hardware interrupt source on the core) not just the core to which it is attached in the project configuration. Therefore the ISR for a CPU interrupt or an INTC1 interrupt should check the core ID of the core on which it is running before carrying out any actions that should only be carried out on a specific core. This behavior allows applications to make use of INTC1 interrupt vectors that are bound to a different hardware interrupt source on each core. Please see the port guide (section 'CPU and INTC1 interrupts in MultiCore') for details.

Workaround

None.



6 Contacting ETAS

6.1 Technical Support

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see Section 6.2.2).

The best way to get technical support is by email. Any problems or guestions about the use of the product should be sent to:

rta.hotline.uk@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- Your .xml, .arxml, .rtaos and/or .stc files
- The command line which caused the error
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The error message you received (if any)
- The file Diagnostic.dmp if it was generated

6.2 **General Enquiries**

6.2.1 **ETAS Global Headquarters**

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6.2.2 ETAS Local Sales & Support Offices

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

> ETAS subsidiaries www.etas.com/en/contact.php ETAS technical support www.etas.com/en/hotlines.php