DRIVING **EMBEDDED EXCELLENCE**

RTA-OS ZynqUSR5/ARM
Release Note - Version 2.0.3 (09-02-2021)

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Safety Notice

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1 Introduction

RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS ZynqUSR5/ARM port plug-in that customizes the RTA-OS development tools for the Xilinx Zynq UltraScale+ Cortex-R5 with the ARM_DS compiler. It supplements the more general information you can find in the *Release Note*.

1.1 Version Information

This is Version 2.0.3 of the RTA-OS ZynqUSR5/ARM plug-in.

1.2 Installation

The installation process is covered in detail in the *ZynqUSR5ARM Port Guide*.

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Introduction

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2   Open EHI Calls

Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.

Open EHI Calls

3   Change History

3.1   Version 2.0.3

Additional Features

The following features have been added to this release:

- Support for ARM 6.6.4 Compiler for Functional Safety, in addition to existing support for the ARM 6.6.2 Compiler.

Modified Features

The following features have been modified in this release:

- Updated compiler options.

- Updated build option for specifying the floating point mode (soft, softfp and hard). Hard is now the default selection.

- Os_Set_Edge_Triggered_x and Os_Set_Level_Sensitive_x macros modified to disable and then re-enable interrupts when called.

Removed Features

No features have been removed from this release.

3.2   Version 2.0.2

Additional Features

The following features have been added to this release:

- Second Full Release.

- Support for the ARM 6.6.2 compiler.

Modified Features

The following features have been modified in this release:

- Port is now compiled with the -mcpu=cortex-r5 option.

- Compiler and linker options have been changed. The port is now compiled with the C99 dialect, and the O2 optimization level. Further options can be seen in the port guide.

- Vector labels have been updated to match the latest version of Zynq UltraScale reference manual. Previous versions of the manual used an incorrect order.

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Change History

Removed Features

The following features have been removed from this release:

- Support for the v6.6 ARM DS-5 compiler.

3.3 Version 2.0.1

Additional Features

The following features have been added to this release:

- First Full Release.

Modified Features

The following features have been modified in this release:

- TrustedWithProtection support has been improved to better handle the enabling and disabling of the MPU in interrupts.

Removed Features

No features have been removed from this release.

3.4 Version 2.0.0 (Preview Release)

Additional Features

The following features have been added to this release:

- Sixth Early Access release.

- Macros to enable, disable and clear GIC interrupts without corrupting the priority.

- Macros to enable and disable all GIC interrupts on a CPU without corrupting the priority.

- Support for the AUTOSAR ISR source API functions (i.e. ClearPendingInterrupt(), DisableInterruptSource() and EnableInterruptSource()).

- MISRA compliance to conform to the MISRA2012 standard.

- FPU support.

- Target option to control the Floating-Point mode used by the compiler.

- Target option to control the Floating-Point registers saved and restored by RTA-OS on ISR or task preemption.

- Tests to alert user if they use interrupts or exceptions that are required by RTA-OS.

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Change History

Modified Features

The following features have been modified in this release:

- Names of the interrupt vectors to match those in v1.7 of the Zynq UltraScale+ Device Technical Reference Manual UG1085.

Removed Features

No features have been removed from this release.

3.5 Version 1.99.4 (Preview Release)

Additional Features

The following features have been added to this release:

- Fifth Early Access release.

- ECC task support.

- Support for memory and timing protection.

- Support for aligning stack to memory protection regions.

- Support for untrusted stack testing in GIC ISRs.

Modified Features

The following features have been modified in this release:

- Tested on a Xilinx UltraScale+ ZCU102 evaluation board using the v6.6 ARM DS-5 compiler.

Removed Features

No features have been removed from this release.

3.6 Version 1.99.3 (Preview Release)

Additional Features

The following features have been added to this release:

- Fourth Early Access release.

- CPU interrupt support.

- Spurious interrupt support.

- Interrupt configuration macros.

Modified Features

The following features have been modified in this release:

- Preliminary GIC interrupt support (tested).

- Tests now run on Xilinx UltraScale+ Silicon instead of a simulator.

Removed Features

No features have been removed from this release.

3.7   Version 1.99.2 (Preview Release)

Additional Features

The following features have been added to this release:

- Third Early Access release.

- Support for v6.6 ARM DS-5 Compiler.

Modified Features

The following features have been modified in this release:

- Preliminary GIC interrupt support (untested).

- Link Type target option to cover On-Chip memory (OCM) and Tightly Coupled Memory (TCM).

- Set interrupt priority range target option.

Removed Features

The following features have been removed from this release:

- Preliminary R-Car x3 Cortex-R7 support.

- Support for v6.3 ARM DS-5 Compiler.

3.8   Version 1.99.1 (Preview Release)

Additional Features

The following features have been added to this release:

- Second Early Access release.

- Preliminary GIC interrupt support (untested).

- Preliminary R-Car x3 Cortex-R7 support (untested).

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Change History

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

3.9 Version 1.99.0 (Preview Release)

Additional Features

The following features have been added to this release:

- Initial Early Access release.

- BCC task support only.

- SC1 AUTOSAR conformance only.

Modified Features

No features have been modified in this release.

Removed Features

No features have been removed from this release.

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Change History

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4   Fixed EHI Calls

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls have been fixed in this release.

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Fixed EHI Calls

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5 Limitations

5.1 Installer

There are the following limitations for the installer:

Limitation	None.
Workaround	None.

5.2 ZynqUSR5ARM DLL

There are the following limitations for this tool:

Limitation	MultiCore operation is not supported.
Workaround	None.

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Limitations

6   Contacting ETAS

6.1   Technical Support

Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see below).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The command line (or reproduction of steps) that result in an error message
- The error messages or return codes you received (if any)
- Your `.xml`, `.arxml` and `.rtaos` files
- The file `Diagnostic.dmp` if it was generated

6.2   General Enquiries

6.2.1   ETAS Global Headquarters

ETAS GmbH

Borsigstrasse 24	Phone:	+49 711 3423-0
70469 Stuttgart	Fax:	+49 711 3423-2106
Germany	WWW:	www.etas.com

6.2.2   ETAS Local Sales & Support Offices

Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

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