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## RTA-OS RH850/GHS

Release Note - Version 5.0.35 (05-09-2022)

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## Safety Notice

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# 1 Introduction

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RTA-OS is an AUTOSAR compliant Operating System and associated tooling. This document provides release information for the RTA-OS RH850/GHS port plug-in that customizes the RTA-OS development tools for the Renesas RH850 with the GREENHILLS compiler. It supplements the more general information you can find in the *Release Note*.

## 1.1 Version Information

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This is Version 5.0.35 of the RTA-OS RH850/GHS plug-in.

## 1.2 Installation

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The installation process is covered in detail in the *RH850GHS Port Guide*.

## 2 **Open EHI Calls**

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Open issues are referred to by their call number in the ETAS Helpdesk International (EHI) system.

No EHI calls are open.

## 3 Change History

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### 3.1 Version 5.0.35

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#### Additional Features

The following features have been added to this release:

- Support for Green Hills frozen version 2022.1.4 compiler tools.
- The target option 'Use GHS headers' when set to TRUE will include the 'v800\_ghs.h' and 'ghs\_barrier.h' header files. The target option defaults to FALSE.

#### Modified Features

The following features have been modified in this release:

- The static qualifier has been added to the inline asm functions OS\_FETRAP\_ENTRY(), OS\_FETRAP\_LEAVE(), os\_trap(), Os\_dbpush\_r10(), Os\_dbpush\_r11() and Os\_GetSP().

#### Removed Features

No features have been removed from this release.

### 3.2 Version 5.0.34

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#### Additional Features

The following features have been added to this release:

- Support for the U2B\_ICUMHB chip variant.

#### Modified Features

The following features have been modified in this release:

- The Enhanced Isolation functionality has been updated so that single core applications can now safely use CallTrustedFunction when ORTI is disabled.

#### Removed Features

No features have been removed from this release.



### 3.3 Version 5.0.33 (Preview Release)

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#### **Additional Features**

The following features have been added to this release:

- Support for the E2M\_ICUMD chip variant.
- This preview is only tested on the E2M\_ICUMD and the GHS v2021.1.5 compiler.
- Support for Green Hills version 2015.1.7 Patch 16 compiler tools.
- When the RTA-OS option 'Omit Default Implementations' is true, then the default implementations of the following functions are not generated: Os\_Cbk\_Idle, Os\_Cbk\_InShutdown, Os\_Cbk\_StackOverrunHook, Os\_Cbk\_StartCore, Os\_Cbk\_StopCore, Os\_AwaitStartup, GetAbortStack and GetEnhancedIsolationStack.

#### **Modified Features**

The following features have been modified in this release:

- An RTAOS.dba file will be generated if target option 'Customer compiler option set 1' or 'Compiler option set 2' is enabled and a source license is present.
- The OS\_NOP() function extern has been moved to avoid a possible conflict with a later declaration.

#### **Removed Features**

No features have been removed from this release.

### 3.4 Version 5.0.32

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#### **Additional Features**

The following features have been added to this release:

- Support for Os\_AwaitStartup. Os\_Cbk\_AwaitStartup and Os\_Cbk\_StopCore are still supported for backwards compatibility.
- Option to control clearing of processor state in Os\_abort 'Abort cleanup'.

### Modified Features

The following features have been modified in this release:

- Updated the declaration for the Enhanced Isolation callbacks `Os_Cbk_IsUntrustedCodeOK`.
- The code used to switch between trusted and trusted-with-protection in the RTA-OS interrupt Category 2 and cross-core wrappers has been made more efficient.
- The `Os_Clear_x` macros have been updated to reduce casting and avoid integer promotion.
- Use of compiler intrinsic functions has been updated to avoid contention with compiler header files.
- The contents of the RTA-OS generated header files have been updated to reduce MISRA deviations, such as multiple declarations of `OS_SELID_0` in some configurations.
- The Category 1 ISR handler function externs are now always generated regardless of whether ORTI is enabled.
- The RTA-OS interrupt and exception assembler support code has been updated to use the 'jr32' instruction rather than the 'jr' instruction to support longer jumps.
- The RTA-OS generated code was checked to ensure that it was not affected by the Renesas errata when 'the result of a write to memory or control register is needed for a subsequent instruction fetch'.

### Removed Features

No features have been removed from this release.

## 3.5 Version 5.0.31

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### Additional Features

The following features have been added to this release:

- Release version with same features as 5.0.30 Preview.

### Modified Features

No features have been modified in this release.

### Removed Features

No features have been removed from this release.

### 3.6 Version 5.0.30 (Preview Release)

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#### **Additional Features**

The following features have been added to this release:

- Supports fast compilation by default. Can be disabled using target option 'No fast compile'.
- Support for the P1M-E chip variant.
- Support for Green Hills version 2021.1.5 compiler tools.
- Support for Green Hills frozen version 2021.1.5 compiler tools.
- Customer Option Set 3. Selectable via the target option 'Compiler option set 3'.
- Double declaration of compiler intrinsics should now be prevented.

#### **Modified Features**

The following features have been modified in this release:

- Os\_EnhancedIsolationStack should now be placeable via MemMap mechanism.
- OS\_MAIN macro modified to have a return type of void.

#### **Removed Features**

No features have been removed from this release.

### 3.7 Version 5.0.29

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#### **Additional Features**

The following features have been added to this release:

- Support for the E2GH\_ICUMD chip variant.
- Support for the E2GUH\_ICUMD chip variant.

#### **Modified Features**

The following features have been modified in this release:

- Renamed the ICUMC, ICUMD and ICUMHA variants to include their host part, P1HC\_ICUMC, F1KM\_ICUMD and U2A\_ICUMHA respectively.
- When ORTI is enabled via the target option, function declaration externs for Cat1 ISRs are generated.
- Updated user guide text.

### Removed Features

The following features have been removed from this release:

- The Os\_EIBDx register definitions for INTC1 are not used and as a result have been removed.

## 3.8 Version 5.0.28

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### Additional Features

The following features have been added to this release:

- Fix for EHI 639880
- Support for Green Hills frozen version 2018.1.5 compiler tools.

### Modified Features

No features have been modified in this release.

### Removed Features

No features have been removed from this release.

## 3.9 Version 5.0.27

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### Additional Features

The following features have been added to this release:

- Fix for EHI 637722.

### Modified Features

The following features have been modified in this release:

- Compiler option set 2 has been updated to more strictly enforce its specified compiler options. The following options are still adjustable via target option: Optimization Strategy, SDA Threshold, and Large SDA.

### Removed Features

No features have been removed from this release.

### 3.10 Version 5.0.26

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#### **Additional Features**

The following features have been added to this release:

- Support for adjusting the ISR stack for Secure Boot compatibility on G3K targets.
- Updated to add fix for EHI issue 635044.

#### **Modified Features**

The following features have been modified in this release:

- The fix for EHI 630139 has been updated to remove the redundant call to `Os_RunCurrentTerminator()`.

#### **Removed Features**

No features have been removed from this release.

### 3.11 Version 5.0.25

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#### **Additional Features**

The following features have been added to this release:

- Support for Green Hills 2019.1.5 compiler tools.

#### **Modified Features**

The following features have been modified in this release:

- Cases where the pragma `ghs nowarning` are used have been modified to correctly re-enable the warning immediately after the affected lines.
- MISRA deviations have been moved closer to the area they apply to, rather than in a separate file.
- The `Os_Cbk_StopCore` macro has been renamed to `Os_Cbk_AwaitStartup` to better reflect its intended function. `Os_Cbk_StopCore` can still be used to preserve backwards compatibility.
- The `memset` and `save/restore stack` functions have been reworked to reduce the number of MISRA deviations.
- Updated to add fix for EHI issue 630139.

#### **Removed Features**

No features have been removed from this release.

### 3.12 Version 5.0.24

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#### **Additional Features**

The following features have been added to this release:

- Full Support for the ICUMHA.
- Multi Debugging Scripts for the ICUMHA.

#### **Modified Features**

No features have been modified in this release.

#### **Removed Features**

No features have been removed from this release.

### 3.13 Version 5.0.23 (Preview Release)

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#### **Additional Features**

The following features have been added to this release:

- Interim Software Only Preview Release.
- Software only support for the ICUMHA chip variant. No tests run on hardware, no support added for sample applications.

#### **Modified Features**

No features have been modified in this release.

#### **Removed Features**

No features have been removed from this release.

### 3.14 Version 5.0.22

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#### **Additional Features**

No features have been added to this release.

#### **Modified Features**

No features have been modified in this release.

#### **Removed Features**

No features have been removed from this release.

### 3.15 Version 5.0.21 (Preview Release)

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#### **Additional Features**

The following features have been added to this release:

- Interim Preview Release.
- Added support for the C1MA2\_CPU1\_CPU2 variant. This is a multicore variant that runs on the CPU1 and CPU2 cores of an RH850/C1M-A2.
- Added support for the C1MA2\_CPU1 variant. This is a single-core variant that runs on the CPU1 core of an RH850/C1M-A2.
- Added support for the C1MA2\_CPU2 variant. This is a single-core variant that runs on the CPU2 core of an RH850/C1M-A2.
- Added support for the C1MA2\_SubCPU variant. This is a single-core variant that runs on the SubCPU core of an RH850/C1M-A2.
- If memory protections callbacks, register sets or timing protection are used, then when a Category 2 interrupt occurs, all Category 2 interrupts are disabled until just before the Category 2 ISR is called. This is to protect OS data structures.

#### **Modified Features**

The following features have been modified in this release:

- The exemplar linker scripts generated now specify the correct CPU type rather than rh850.
- Corrects the way that `Os_InitializeVectorTable()` writes to EIBDn registers so that the GPID field is set correctly.

#### **Removed Features**

No features have been removed from this release.

### 3.16 Version 5.0.20

---

#### **Additional Features**

The following features have been added to this release:

- Support for the ICUMXA chip variant

### Modified Features

The following features have been modified in this release:

- Option set 2 no longer includes the -nofloatio and -brief\_diagnostics options
- Os\_TerminateApplication() has been updated to avoid a compilation error when enhanced isolation is used and applications are terminated.
- Updated to add fix for EHI issue 598708.

### Removed Features

No features have been removed from this release.

## 3.17 Version 5.0.19

---

### Additional Features

The following features have been added to this release:

- Support for Green Hills 2018.1.5 compiler tools in addition to the 2017.1.5, Patch 42 v2013.5.5 and Patch 11 v2015.1.7 compiler tools
- Target option to select a second alternative compiler option set
- Trusted with protection applications are now supported in SC1 configurations

### Modified Features

The following features have been modified in this release:

- Cross-core interrupt handlers now have per-core implementations, which improves cross-core interrupt performance

### Removed Features

No features have been removed from this release.

## 3.18 Version 5.0.18

---

### Additional Features

The following features have been added to this release:

- Eleventh Full Multicore Release.
- Support for the F1KH chip variant.
- Support for the ICUMD chip variant.



### Modified Features

The following features have been modified in this release:

- Update support for the ICUMC chip variant.

### Removed Features

No features have been removed from this release.

## 3.19 Version 5.0.17 (Preview Release)

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### Additional Features

The following features have been added to this release:

- Interim Preview Release.
- Support for the F1KM chip variant (i.e. covers both the F1KM-S1/F1KM-S4).
- The target option 'Unaligned data' has been added to control the use of the -misalign\_pack/-no\_misalign\_pack compiler option.
- Support for Trusted-with-Protection.
- Tests are now made to determine possible conflicts between configured interrupts and any interrupts required by the OS.
- Support for the Autosar ISR source API functions (i.e. ClearPendingInterrupt(), DisableInterruptSource() and EnableInterruptSource()).

### Modified Features

The following features have been modified in this release:

- Support for Green Hills 2017.1.5 compiler tools in addition to the Patch 42 v2013.5.5 compiler and Patch 11 v2015.1.7 compiler tools.
- The 'Optimizer setting' target option now supports the use of Onone
- MISRA compliance updated to conform to the MISRA2012 standard.
- In multicore configurations that use the cached CoreID target the interrupt APIs have been updated so that they can be safely used before StartOS() (i.e. EnableAllInterrupts()/DisableAllInterrupts(), SuspendAllInterrupts()/ResumeAllInterrupts(), SuspendOSInterrupts()/ResumeOSInterrupts()).
- In multicore configurations where only the master core is running an AUTOSAR OS and only the master core uses interrupts Os\_InitializeVectorTable() has been updated so that only the master core configures the interrupts.
- Updated to add fix for EHI issues 567360 and 550149.

### Removed Features

No features have been removed from this release.

## 3.20 Version 5.0.16

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### Additional Features

The following features have been added to this release:

- Eleventh Full Multicore Release.
- Support for the P1L-C chip variant.

### Modified Features

The following features have been modified in this release:

- Support for Patch 41 Green Hills v2013.5.5 compiler tools in addition to the Patch PO8 v2015.1.7 compiler tools.
- Tested on the G3K, G3KH and G3M chip variants using Green Hills Compiler compiler versions v2013.5.5 (patch 41) and v2015.1.7 (patch PO8).
- Updated to add fix for EHI issue 544626.

### Removed Features

No features have been removed from this release.

## 3.21 Version 5.0.15

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### Additional Features

The following features have been added to this release:

- Tenth Full Multicore Release.

### Modified Features

The following features have been modified in this release:

- Completes support for the D1x chip variants (i.e. D1L1, D1L2(H), D1M1(H), D1M2(H)).
- Tests now complete for the 'Enhanced Isolation' support.
- Support for Patch PO8 Green Hills v2015.1.7 compiler tools in addition to the Patch 2 v2013.5.5 compiler tools.
- Tested on the G3K, G3KH and G3M chip variants using Green Hills Compiler compiler versions v2013.5.5 (patch 2) and v2015.1.7 (patch PO8).

- Updated Lauterbach Trace32 to release version R.2016.02.000072893.
- Updated to add fix for EHI issue 534608.

### Removed Features

No features have been removed from this release.

## 3.22 Version 5.0.14 (Preview Release)

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### Additional Features

The following features have been added to this release:

- Interim Preview Release.
- Initial support for the D1x chip variants (i.e. D1L1, D1L2(H), D1M1(H), D1M2(H)).

### Modified Features

The following features have been modified in this release:

- Minor changes have been applied to the abort handler for applications that use 'Enhanced Isolation' (EI).

### Removed Features

No features have been removed from this release.

## 3.23 Version 5.0.13 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Interim Preview Release.

### Modified Features

The following features have been modified in this release:

- The 'Enhanced Isolation' (EI) support now supports multi-core applications. The EI stack is no longer configured using a banked label, instead pointers are initialized during StartOS(). The default stack of 400 bytes per core can be overridden by the callback function Os\_Cbk\_GetEnhancedIsolationStack(). The variable Os\_LastProtectionFault is now updated when untrusted code is terminated by EI. Please refer to the 'RTA-OS RH850GHS Port Guide' for further details.
- The code to support the 'enable stack repositioning' target option has been updated. When dealing with Tasks, untrusted functions and untrusted hooks both the repositioned and normal code no longer relies on values stored in the CPU general purpose registers to be preserved over the call to untrusted code.

### Removed Features

No features have been removed from this release.

## 3.24 Version 5.0.12 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Interim Preview Release.
- The target option 'Enhanced Isolation' has been added to prevent any faulty untrusted code from affecting the operation of trusted code. Faulty untrusted code can be terminated without having to shutdown the rest of the system. The initial implementation is for demonstration purposes and is currently only supported in single core applications. Please refer to the 'RTA-OS RH850GHS Port Guide' for further details.

### Modified Features

The following features have been modified in this release:

- Minor updates to the header file compiler.h.
- The compiler option set now includes '-lnk=-no\_xda\_modifications'

### Removed Features

No features have been removed from this release.

## 3.25 Version 5.0.11

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### Additional Features

The following features have been added to this release:

- Ninth Full Multicore Release.

### Modified Features

The following features have been modified in this release:

- Minor updates to the RH850 port guide.

### Removed Features

No features have been removed from this release.

### 3.26 Version 5.0.10 (Preview Release)

---

#### **Additional Features**

The following features have been added to this release:

- Interim Preview Release.
- Support for the F1K chip variant.
- Support for the setting the interrupt priority level of the FPI/FPP interrupt in G3KH core variants.
- The target option 'stack\_protector setting' has been added to support the use of the -stack\_protector compiler option.
- Support for Green Hills v2015.1.7 compiler tools in addition to the Patch 2 v2013.5.5 compiler tools.

#### **Modified Features**

The following features have been modified in this release:

- Multicore applications that have either stack or timing execution measurement enabled could erroneously configure the cross-core ISRs to have the highest priority. This has now been corrected so that they only ever have the lowest priority.
- Updated to add fix for EHI issue 513992
- Tested on the G3K, G3KH and G3M chip variants using Green Hills Compiler compiler versions v2013.5.5 (patch 2) and v2015.1.7.

#### **Removed Features**

The following features have been removed from this release:

- Support for Green Hills v2015.1.5 compiler tools

### 3.27 Version 5.0.9

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#### **Additional Features**

The following features have been added to this release:

- Eighth Full Multicore Release.
- A target option to select a customer compiler option set has been added. When selected tests are applied to ensure that all target options are compatible with the compiler option set.
- Support for a single cross-core interrupt (IPIR) channel used by all cores. Selected via the existing cross-core target options (CrossCore0 IPIR and CrossCore1 IPIR).

### Modified Features

The following features have been modified in this release:

- Now supports both the Patch 2 Green Hills v2013.5.5 and the v2015.1.5 compiler tools.
- Updated the cross-core interrupt code to remove unnecessary core check.
- Updated the RH850GHS port guide to add details on the cross-core interrupt support.
- Updated the RH850GHS port guide to add details on the TRAP, FETRAP and SYSCALL support.
- Updated to add fix for EHI issue 495718
- Tested on the G3K single core core (R1L, F1L), the G3M single core (E1L, F1M, P1M, P1M-C), and the G3M multicore (F1H, P1H-C) chip variants.

### Removed Features

The following features have been removed from this release:

- Support for Green Hills v2014.5.5 compiler tools

## 3.28 Version 5.0.8 (Preview Release)

### Additional Features

The following features have been added to this release:

- Interim Preview Release.
- Support for iSYSTEM User Tracing
- Support for the E1L, E1M-S, P1M chip variants.
- Test in StartOS so that the FPU target option cannot be used on the E1x core without an FPU.
- Add noline and noreturn attributes to `os_longjmp()` and the untrusted stack alignment support code to guarantee the compiler never inlines this code.
- Add `syncp` instructions to the vector table interrupt entries for G3M cores to address a reported issue from Renesas.

### Modified Features

The following features have been modified in this release:

- Rework the OS API code when used in applications with untrusted objects to avoid unnecessary use of a function callout when restoring the trust mode at the end of the API code.
- Tested on the G3K single core core (F1L), the G3M single core (F1M, P1M-C), and the G3M multicore (F1H, P1H-C) chip variants.

### Removed Features

No features have been removed from this release.

## 3.29 Version 5.0.7

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### Additional Features

The following features have been added to this release:

- Seventh Full Multicore Release.
- Os\_INTChannel\_x macros.
- Support for the E1L and E1M-S chip variants.
- The target option 'Cache CoreID in CTPSW' has been added to improve the performance of detecting the core ID in multicore applications.
- P1H-C now tested on the R7F701327 D4 part (based upon the D5EDv2 architecture). See the limitations section for more details.

### Modified Features

The following features have been modified in this release:

- Now supports both the Patch 2 Green Hills v2013.5.5 and the v2014.5.5 compiler tools.
- The GHS \_\_memory\_changed() memory barrier optimization intrinsic function has been placed around other intrinsic functions to prevent instruction re-ordering when aggressive optimization levels are applied by the compiler command line options.
- Updated the default implementation of Os\_Cbk\_GetAbortStack() so that no stack is used in both single and multicore applications.
- The code to support the 'enable stack repositioning' target option has been updated. The assembly language instructions generated now do not rely on values stored in the CPU general purpose registers to be preserved over the call to untrusted code.

- The support for stack and execution time measurement has been updated to prevent a possible miscalculation when a higher priority Category 2 interrupt occurs during the calculations.
- The code in `Os_longjmp` updated to protect against ISRs when the `longjmp` buffer is on the stack (only affects ECC tasks when 'Enable stack repositioning' is selected).
- Details on the `Os_Cbk_GetAbortStack()` callback now added to the documentation.
- Rework the OS Size Information support code (`gdump` strings) in the generated interrupt vector table to simplify the module size calculations.
- P1M-C support now fully tested on hardware.

### Removed Features

No features have been removed from this release.

## 3.30 Version 5.0.6

---

### Additional Features

The following features have been added to this release:

- Sixth Full Multicore Release.
- Support for the P1H-C chip variants (tested on hardware). This will replace the CCC variant which will be removed in a future release.

### Modified Features

The following features have been modified in this release:

- P1H-C interrupt vector labels are updated to match the latest documentation.
- P1M-C interrupt vector labels are updated to match the latest documentation.
- User Guide text updated to include information on the highest interrupt vector in the vector table generated by RTA-OS when using Table Reference Interrupt vectors.
- The untrusted stack check tests are now fully implemented and tested. These make sure that no stack is used before the stack has been safely tested.

### Removed Features

No features have been removed from this release.



### 3.31 Version 5.0.5 (Preview Release)

---

#### **Additional Features**

The following features have been added to this release:

- Interim Preview Release.
- Support for the F1M and P1M-C chip variants.

#### **Modified Features**

The following features have been modified in this release:

- Updated the default implementation of `Os_Cbk_GetAbortStack()` so that no stack is used in both single and multicore applications.

#### **Removed Features**

No features have been removed from this release.

### 3.32 Version 5.0.4

---

#### **Additional Features**

The following features have been added to this release:

- Fifth Full Multicore Release.
- Link time optimization now supported and tested (i.e. linker command line options `-delete` and `-ignore_debug_references`)

#### **Modified Features**

The following features have been modified in this release:

- R1L interrupt vector labels are updated to match the latest documentation.
- Target option to set the EBASE/RBASE registers updated to remove the RBASE register configuration as this cannot be changed at runtime.
- If the PIE interrupt (0xA0) is unconfigured the generated vector table entry is now always routed to `Os_abort()` even when the default interrupt is selected.

#### **Removed Features**

No features have been removed from this release.

### 3.33 Version 5.0.3

---

#### **Additional Features**

The following features have been added to this release:

- Fourth Full Multicore Release.

#### **Modified Features**

The following features have been modified in this release:

- The build options have been modified to prevent a warning from being generated for `Os_Wrapper.c`.

#### **Removed Features**

No features have been removed from this release.

### 3.34 Version 5.0.2

---

#### **Additional Features**

The following features have been added to this release:

- Third Full Multicore Release.

#### **Modified Features**

The following features have been modified in this release:

- The exception codes are now passed to the `Os_abort` trap handler using `r29` rather than `r6` to protect the value during user supplied versions of `Os_Cbk_GetAbortStack()` when used.

#### **Removed Features**

No features have been removed from this release.

### 3.35 Version 5.0.1

---

#### **Additional Features**

The following features have been added to this release:

- Second Full Multicore Release.
- Support for the C1H and C1M chip variants (not tested on hardware).
- Target option to allow user selection of the SDA address offset (23-bit or 16-bit).
- Target option to allow the default interrupt to be run at a low IPL.
- Target option to always use `Os_Cbk_GetAbortStack()` to set up a safe area of memory to use as a stack when executing the ProtectionHook.

#### **Modified Features**

The following features have been modified in this release:

- The `Os_abort` trap handler used when calling the ProtectionHook has been modified to use less stack and not use stack before calling `Os_Cbk_GetAbortStack()` when applicable.

#### **Removed Features**

No features have been removed from this release.

### 3.36 Version 5.0.0

---

#### **Additional Features**

The following features have been added to this release:

- First Full Multicore Release.
- Test that FPU target option cannot be selected for use on a variant without an FPU on all cores.
- Target option to allow user selection of cross core interrupts.

#### **Modified Features**

The following features have been modified in this release:

- F1H variant now fully tested.
- Moved compiler to only support the Patch 2 Green Hills v2013.5.5 tools.
- Rework the OS Size Information support to correct module size calculations and to report size of assembler modules in the OS library.

### Removed Features

No features have been removed from this release.

## 3.37 Version 4.99.4 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Fifth Early Access Multicore Release, and no warranty is provided for use in production applications.
- Support for the F1H chip variant (not tested).
- Target option to support handling of FPU context.

### Modified Features

The following features have been modified in this release:

- Reduced transition time of ECC tasks entering and leaving the waiting state.
- Compiler option `-large_sda` replaced with `-no_large_sda` as this gives improved code size.

### Removed Features

No features have been removed from this release.

## 3.38 Version 4.99.3 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Fourth Early Access Multicore Release, and no warranty is provided for use in production applications.

### Modified Features

The following features have been modified in this release:

- Moved compiler to only support the Green Hills v2013.5.5 tools.
- CPU compiler option modified for variant core type.
- Use of default interrupt with untrusted applications now supported.
- Sample applications now supported by the CCC-D5ED variant.
- ORTI now supported on multicore applications.
- Partially tested on the Renesas CCC-D5ED silicon, fully tested on the F1L silicon.

### Removed Features

The following features have been removed from this release:

- Support for the Green Hills v2013.1.5 compiler tools.

## 3.39 Version 4.99.2 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Third Early Access Multicore Release, and no warranty is provided for use in production applications.

### Modified Features

The following features have been modified in this release:

- Visibility of defines used in core identification.
- Use of compiler intrinsic functions.

### Removed Features

No features have been removed from this release.

## 3.40 Version 4.99.1 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Second Early Access Multicore Release, and no warranty is provided for use in production applications.
- Multicore support for Direct Vector method interrupt vectors.
- First Early Access Multicore Release, and no warranty is provided for use in production applications.

### Modified Features

The following features have been modified in this release:

- Removal of dependency of T32 environment variable.
- ORTI support modified for multicore applications.
- Partially tested on the Renesas SCIT-CCC-D5ED S2-R05 bitstream.

### Removed Features

No features have been removed from this release.

## 3.41 Version 4.99.0 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Support for the CCC-5DED chip variant (as CCC).
- Multicore support for multicore variants (i.e. E1x-FCC, CCC-5DED).

### Modified Features

The following features have been modified in this release:

- Partially tested on the Renesas E1x-FCC.

### Removed Features

No features have been removed from this release.

## 3.42 Version 2.0.0

---

### Additional Features

The following features have been added to this release:

- First Full Release.
- Added support for raw exception handlers for CPU exceptions.
- Added support for FEINT interrupt in the abort handler.
- Added macros to enable and disable all the maskable interrupt channels together without corrupting the priority.

### Modified Features

The following features have been modified in this release:

- Moved compiler to only support the Green Hills v2013.1.5 tools.
- Tested on the Renesas E1x-FCC, R1L and F1L silicon.
- Details added to the user guide on raw exception handlers and default interrupt usage.

### Removed Features

The following features have been removed from this release:

- Support for the F1A FPGA development variant
- Support for the Green Hills v2012.5.5 compiler tools.

## 3.43 Version 1.99.4 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Fifth Early Access Release, and no warranty is provided for use in production applications.
- Added target option to support user configuration of the EBASE/RBASE registers.

### Modified Features

The following features have been modified in this release:

- Corrects support of the FEINT interrupt.
- Corrects support for the F1x-FCC and E1x-FCC1 EI interrupt channels 0 to 31.
- Corrects EI priority initialization for G3K core to use 3 bit values rather than 4.
- Tested on the Renesas E1x MSEVRH850BW and SCIT board programmed with the v1.02 RH850/F1A Bitstream.
- Details added to the user guide on mapping of RH850 IPLs to RTA-OS IPLs.
- Additional details added to the user guide on the CAT1\_ISR macro.

### Removed Features

No features have been removed from this release.

## 3.44 Version 1.99.3 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Fourth Early Access Release, and no warranty is provided for use in production applications.
- Support for G3M cores.
- Support for E1x-FCC (CPU core only), E1x-FCC1(CPU core only), F1L, Generic 8 IPL and Generic 16 IPL variants.
- Added target option to allow use of the SDA.

### Modified Features

The following features have been modified in this release:

- Compiler options updated to only use registermode=32.
- ORTI support modified to also trace CPU traps and exceptions.
- Improved the interrupt support macros to use the interrupt name or channel number.
- Tested on the Renesas E1x MSEVRH850BW and SCIT board programmed with the v1.02 RH850/F1A Bitstream.
- IPL changing code modified to avoid missed scheduling points found when testing on silicon rather than the Bitstream.

### Removed Features

No features have been removed from this release.

## 3.45 Version 1.99.2 (Preview Release)

---

### Additional Features

The following features have been added to this release:

- Third Early Access Release, and no warranty is provided for use in production applications.
- Support for timing and memory protection.
- Support for aligning stack to memory protection regions.
- Support for untrusted stack testing.
- Support for Direct Vector method interrupt vectors.

### Modified Features

No features have been modified in this release.

### Removed Features

No features have been removed from this release.



### 3.46 Version 1.99.1 (Preview Release)

---

#### **Additional Features**

The following features have been added to this release:

- Second Early Access Release, and no warranty is provided for use in production applications.
- Support for Category 1 CPU (EI and FE) exceptions and interrupts (i.e. vector addresses 0x10 to 0xF0).
- Macros to enable, disable and clear interrupt sources without corrupting the priority.

#### **Modified Features**

The following features have been modified in this release:

- Moved compiler to only support the Green Hills v2012.5.5 tools.
- Tested on the Renesas SCIT board programmed with the v1.02 RH850/F1A Bit-stream.

#### **Removed Features**

The following features have been removed from this release:

- Support for the Green Hills v2012.5.1 compiler tools.

### 3.47 Version 1.99.0 (Preview Release)

---

#### **Additional Features**

The following features have been added to this release:

- Initial Early Access. Category 1 and 2 interrupts (Table reference method only). BCCx/ECCx Tasks. SC1 Autosar conformance. RTA-TRACE support

#### **Modified Features**

No features have been modified in this release.

#### **Removed Features**

No features have been removed from this release.

## 4 Fixed EHI Calls

---

Bugs that have been fixed are referred to by their call number in the ETAS Helpdesk International (EHI) system.

### 4.1 Version 5.0.30 (Preview Release)

---

#### **EHI 672801**

*Status:* Fixed

*Title:* Possible trap with a Trusted-with-protection (TWP) and untrusted Application and ECC task.

*Description:* If there is a Trusted-with-protection (TWP) and untrusted OS Application and an untrusted ECC task, then the code in the DispatchECC function tries to disable the MPU while still untrusted, which it is unable to do because it must first be trusted.

#### **EHI 673128**

*Status:* Fixed

*Title:* Compilation error in Os\_CrossCore.c

*Description:* RTA-OS 6.2.0 introduced a code optimization that was not compatible with previous versions of this port.

### 4.2 Version 5.0.29

---

#### **EHI 654720**

*Status:* Fixed

*Title:* Potential compilation build error in IOC multicore applications that use stack repositioning.

*Description:* In some multicore applications using the IOC and the 'Enable stack repositioning' target option, a compilation error can occur in CallTrustedFunction.c. This release has updated the stack alignment support to prevent this.

### 4.3 Version 5.0.28

---

#### **EHI 639880**

*Status:* Fixed

*Title:* Os\_Clear\_x macro is not protected against interrupts that may modify the same register.

*Description:* The Os\_Clear\_x macro compiles to a set of read-modify-write instructions. It is possible that after the initial read, an interrupt could be taken that modifies the previously read register. When the interrupt returns and the modify-write section of the macro is performed, an incorrect value could be written back. To fix this interrupts are disabled around the clear macro. Other interrupt macros are not affected as they do not use the same read-modify-write set of instructions.

#### 4.4 Version 5.0.27

---

##### **EHI 637722**

*Status:* Fixed

*Title:* Do not allow target options to affect compiler options once option set 2 has been configured.

*Description:* With option set 2 selected, compiler options selectable by target option are now ignored and not included if they are not present in option set 2 or marked configurable. A warning is emitted when this occurs.

#### 4.5 Version 5.0.26

---

##### **EHI 635044**

*Status:* Fixed

*Title:* Declaration of `os_current_core` causing a compilation failure due to no reference.

*Description:* In some configurations `os_current_core` would be declared but never referenced in `CallTrustedFunction.c` due to a fix for a previous EHI. This release has been updated to prevent the declared but never referenced error.

#### 4.6 Version 5.0.25

---

##### **EHI 630139**

*Status:* Fixed

*Title:* Enhanced isolation should protect against any register corruption in untrusted code.

*Description:* In `CallTrustedFunction` (when used to call an untrusted function) a line of code between the function call and termination has been shown to use one of the potentially corrupted registers when a multi-core configuration is used. Single core applications did not exhibit this behavior. This release has been updated to prevent the use of the corrupted registers in the above situation.

#### 4.7 Version 5.0.20

---

##### **EHI 598708**

*Status:* Fixed

*Title:* Failure to disable/restore MPU in interrupts when Trusted-WithProtection OS Applications exist

*Description:* The MPU has to be enabled and disabled appropriately to support TrustedWithProtection on the RH850. The code to do this was omitted in Category 2 and cross-core interrupt handlers. This could result in the handler code wrongly running with the MPU enabled, which might result in incorrect memory traps. Alternatively it could result in the MPU being disabled when returning to pre-empted code. This release has been updated to ensure that the MPU is correctly applied.

#### 4.8 Version 5.0.17 (Preview Release)

---

##### **EHI 550149**

*Status:* Fixed

*Title:* Incorrect calls to `Os_Cbk_Terminated_ISRName`

*Description:* In applications that support the forced termination of ISRs the termination call-back is incorrectly called when an untrusted ISR terminates normally. This occurs when the RTA-OS library is built with tools later than v5.4.3. The call-back is not called incorrectly when stack repositioning is enabled or when both timing protection is disabled and `TerminateApplication` is omitted. This release has been updated to prevent the incorrect calls.

##### **EHI 567360**

*Status:* Fixed

*Title:* P1MC incorrect vector name

*Description:* The vector label used to configure interrupt channel 238 for the P1HC/P1MC variants is incorrectly named `FENTRYC_FICUIF_0` when it should be `FENTRYD_FICUIF_0`. This is now corrected.

#### 4.9 Version 5.0.16

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##### **EHI 544626**

*Status:* Fixed

*Title:* iSYSTEM winIDEA User-Trace support for applications with untrusted code and the ShutdownHook and ProtectionHook

*Description:* The macros used to support tracking ORTI items with the iSYSTEM winIDEA profiler User-Trace caused a build error in applications with untrusted code and the ShutdownHook and ProtectionHook. This release has updated the use of these macros to correct this issue. Additional tests have been added to cover all possible use cases for these macros.

#### 4.10 Version 5.0.15

---

##### **EHI 534608**

*Status:* Fixed

*Title:* Braces required around macro parameters

*Description:* The macros used to support tracking ORTI items with the iSYSTEM winIDEA profiler User-Trace did not include sufficient braces. The measured trace data could be incorrect as these macros would not generate correct code for all C pre-processor expansions. This release has updated the macros to correct this issue.

#### 4.11 Version 5.0.10 (Preview Release)

---

##### **EHI 513992**

*Status:* Fixed

*Title:* RH850 EIBD.GPID register not initialized

*Description:* In multicore RH850 applications, the EIBD.GPID values must be initialized such that the appropriate core IDs are given. This release has updated the interrupt initialization code within `Os_InitializeVectorTable()` to ensure that the EIBD.GPID values are set to match the application configuration.

#### 4.12 Version 5.0.9

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##### **EHI 495718**

*Status:* Fixed  
*Title:* Default RTA-OS Os\_Cbk\_GetAbortStack() code can return NULL  
*Description:* In configurations that use the Os\_Cbk\_SetMemoryAccess callback to update the memory protection settings for untrusted code, but where the stack value is not actually passed to the callback (i.e. Stack Monitoring is disabled AND target option 'Enable stack repositioning' is false) a NULL value can be returned. This release has updated the default implementation of Os\_Cbk\_GetAbortStack() to fix this issue.

#### 4.13 Version 5.0.4

---

##### **EHI 422922**

*Status:* Fixed  
*Title:* Missing R1L interrupt vector names in RTA-OS RH850/GHS port  
*Description:* The interrupt vector names have been updated to match the latest documentation.

#### 4.14 Version 4.99.3 (Preview Release)

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##### **EHI 370770**

*Status:* Fixed  
*Title:* Compiler version is not reported in the application build information  
*Description:* The build output now describes the compiler tools version details rather than the IDE version details.

##### **EHI 370771**

*Status:* Fixed  
*Title:* Updated GHS variant options must be used  
*Description:* The CPU compiler option is now updated to use the value for the target variant (i.e. rh850g3k/rh850g3m/rh850g3h) rather than the more generic rh850.

##### **EHI 378794**

*Status:* Fixed  
*Title:* Default interrupt must not overwrite protection exception vectors  
*Description:* In SC3/SC4 configurations the use of default interrupt with untrusted applications is now supported.

## 5 Limitations

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### 5.1 Installer

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There are the following limitations for the installer:

<b>Limitation</b>	None.
<b>Workaround</b>	None.

### 5.2 RH850GHS DLL

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There are the following limitations for this tool:

<b>Limitation</b>	iSYSTEM debugger ORTI support added but not tested.
<b>Workaround</b>	None.

<b>Limitation</b>	Tests running applications on the D5EDv2 hardware found a limitation with multicore applications. If both code and data located in GRAM then the GRAM Write-Through buffer must be disabled otherwise there is an issue with code coherency between cores. If code is located in internal FLASH and data in GRAM then the Write-Through buffer can be used safely. This has been fixed in the D5EDv3 silicon.
<b>Workaround</b>	None.

<b>Limitation</b>	A silicon errata exists affecting the following devices with a G3M core: RH850/E1x-FCC1, E1L, E1M-S, P1L-C, P1M-C, P1H-C, P1M, P1M-E, C1H, C1M, D1x, F1H, F1M, whereby it's possible that an EI or EIINT exception that is immediately pre-empted by a higher priority exception (FEINT, SYSERR, FENMI or FPI) using the table reference method, could incorrectly jump to the EIINT handler. The following other conditions also have to be met in order for this issue to be applicable. The table and any other instructions/data must be allocated in ROM, the CPU frequency must be less than or equal to 160MHz and any other bus master (other CPU, PCU, ICUM, DMAC etc.) that accesses the Flash bank that the G3M CPU also accesses. There are several workarounds for this silicon errata including using direct vectoring for EIINT interrupts, locating the vector table in LRAM or GRAM, disabling the acceleration of the ROM table reference method EIINT or inserting a detection routine into the EIINT and EI level exception handlers. Please contact Renesas for further details.
<b>Workaround</b>	None.

## 6 Contacting ETAS

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### 6.1 Technical Support

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Technical support is available to all users with a valid support contract. If you do not have a valid support contract, please contact your regional sales office (see below).

The best way to get technical support is by email. Any problems or questions about the use of the product should be sent to:

rta.hotline@etas.com

If you prefer to discuss your problem with the technical support team, you call the support hotline on:

+44 (0)1904 562624.

The hotline is available during normal office hours (0900-1730 GMT/BST).

In either case, it is helpful if you can provide technical support with the following information:

- Your support contract number
- The version of the ETAS tools you are using
- The version of the compiler tool chain you are using
- The command line (or reproduction of steps) that result in an error message
- The error messages or return codes you received (if any)
- Your .xml, .arxml and .rtaos files
- The file Diagnostic.dmp if it was generated

### 6.2 General Enquiries

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#### 6.2.1 ETAS Global Headquarters

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**ETAS GmbH**

Borsigstrasse 24  
70469 Stuttgart  
Germany

Phone: +49 711 3423-0  
Fax: +49 711 3423-2106  
WWW: [www.etas.com](http://www.etas.com)

#### 6.2.2 ETAS Local Sales & Support Offices

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Contact details for your local sales office and local technical support team (where available) can be found on the ETAS web site:

ETAS subsidiaries [www.etas.com/en/contact.php](http://www.etas.com/en/contact.php)  
ETAS technical support [www.etas.com/en/hotlines.php](http://www.etas.com/en/hotlines.php)